www.ablic.com

PROGRAMMABLE, FAST-RESPONSE, LINEAR HALL EFFECT SENSOR IC

This IC, developed by CMOS technology, is a programmable fast-response linear Hall effect sensor IC. It provides an analog output voltage proportional to the magnetic flux density based on the VREF pin voltage.
The IC has a built-in non-volatile memory and a 2-wire serial interface that allow flexible switching functions and trimming adjustments. Switching functions are available for the reference voltage operation mode, reference voltage output, output voltage polarity, frequency bandwidth, and thermal shutdown. High-precision trimming adjustments are available for sensitivity, sensitivity thermal drift, output offset voltage, and reference voltage output.
Because of its fast response, it is ideal for current sensor applications such as monitoring instantaneous overcurrent.

■ Features

- Output response time: 2.5 µs max. (frequency bandwidth 400 kHz)
- Analog voltage output proportional to magnetic flux density:
  Operates with VREF pin voltage reference, non-linearity ±0.5% max.
  High resistance to power supply noise due to non-ratiometric operation
- Built-in non-volatile memory: 2-wire serial interface enables switching of IC functions and trimming adjustment
- Built-in thermal shutdown circuit: Detection temperature 170°C typ.
- Switching functions
  - Reference voltage operation mode: Reference voltage output mode*1, reference voltage input mode
  - Reference voltage output: 0.50 V, 1.50 V, 1.65 V, 2.50 V*1
  - Output voltage polarity: Normal polarity*1, opposite polarity
  - Frequency bandwidth: 100 kHz, 200 kHz, 400 kHz*1
  - Thermal shutdown: Available*1, unavailable
- Trimming adjustment
  - Sensitivity: 6 V/T to 180 V/T (130 V/T typ.*1), 0.3% step max.
  - Sensitivity thermal drift: -500 ppm/°C to +500 ppm/°C (0 ppm/°C typ.*1), 25 ppm/°C step typ.
  - Output offset voltage: 1.5 mV step max.
  - Reference voltage output: 4.0 mV step max.
- Power supply voltage range: V_{DD} = 4.5 V to 5.5 V
- Current consumption: I_{DD} = 19 mA typ.
- Operation temperature range: Ta = -40°C to +125°C
- Lead-free (Sn 100%), halogen-free

***1.** Initial settings at shipment

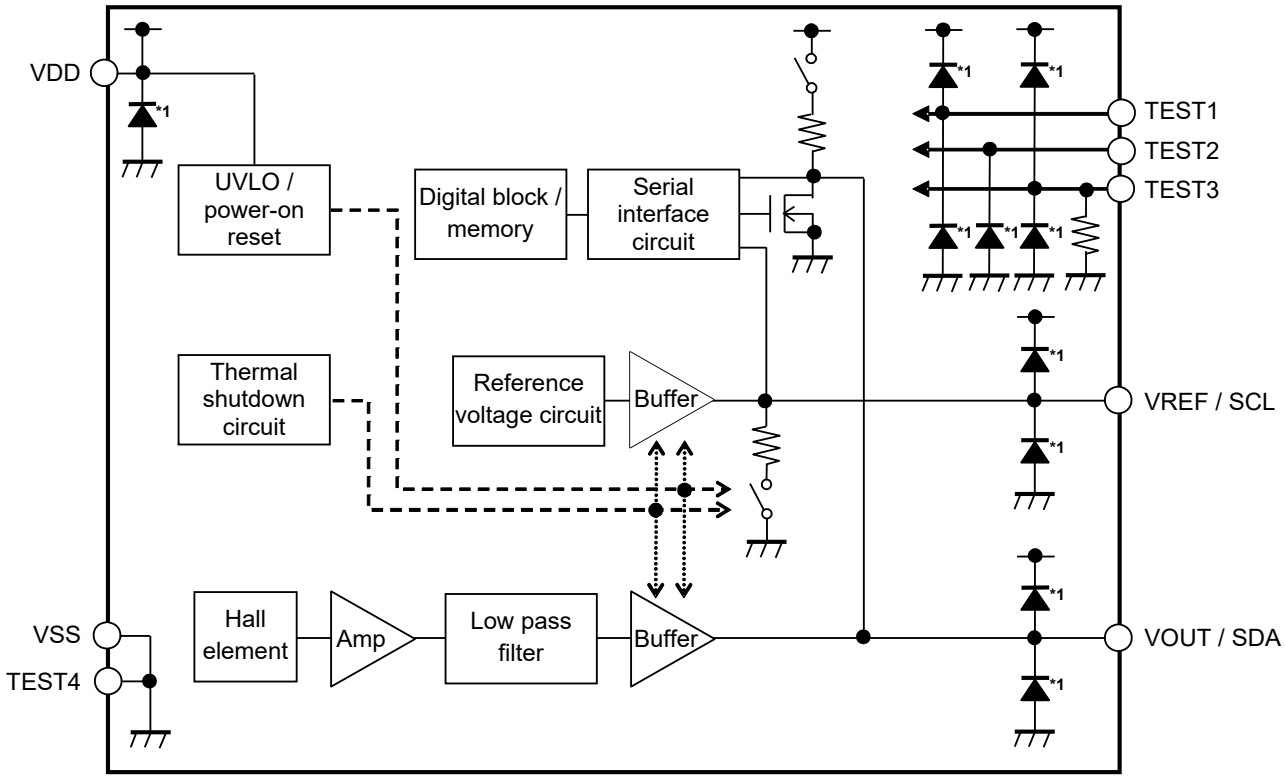
■ Application

- Magnetic core current sensor
- Linear position detection
- Rotation detection

■ Package

- TMSOP-8

■ Block Diagram



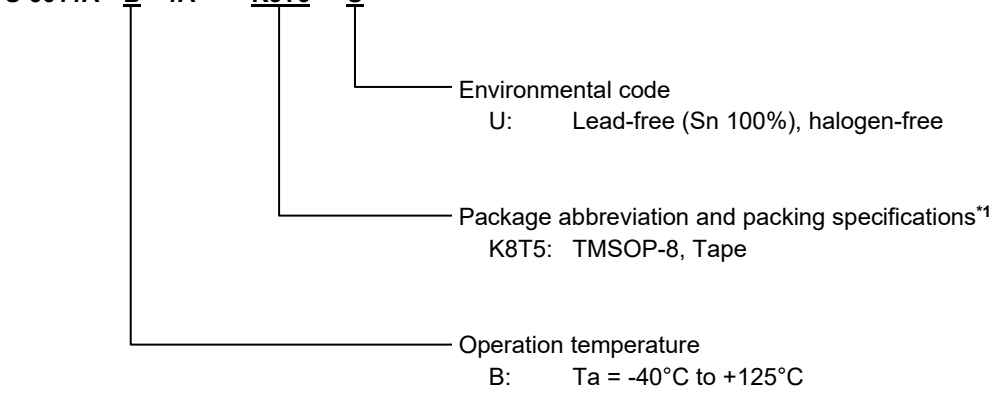
***1.** Parasitic diode

Figure 1

■ Product Name Structure

1. Product name

S-5611A B 1A - K8T5 U



***1.** Refer to the tape drawing.

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD

3. Product name list

Table 2

Product Name	Package
S-5611AB1A-K8T5U	TMSOP-8

■ Pin Configurations

1. TMSOP-8

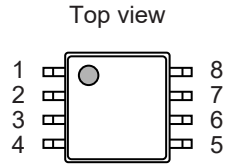


Figure 2

Table 3

Pin No.	Symbol	Description	
1	VREF / SCL*1	VREF	Reference voltage I/O pin
		SCL	Serial clock input pin
2	VOUT / SDA*2	VOUT	Output pin
		SDA	Serial data I/O pin
3	VSS	GND pin	
4	TEST4*3	Test 4 pin	
5	VDD	Power supply pin	
6	TEST1*4	Test 1 pin	
7	TEST2*4	Test 2 pin	
8	TEST3*4	Test 3 pin	

***1.** The VREF / SCL pin combines the reference voltage I/O pin and the serial clock input pin.
***2.** The VOUT / SDA pin combines the output pin and the serial data I/O pin.
***3.** The TEST4 pin is shorted to the VSS pin (refer to **Figure 1**). Set the TEST4 pin open in use.
***4.** Set the TEST1 pin, the TEST2 pin, and the TEST3 pin open in use.

■ Absolute Maximum Ratings

Table 4

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Power supply voltage	V_{DD}	VDD	V_{SS} - 0.3 to V_{SS} + 6.5	V
Input / output voltage	V_{REF}	VREF / SCL	V_{SS} - 0.3 to V_{DD} + 0.3	V
	V_{SCL}	VREF / SCL	V_{SS} - 0.3 to V_{DD} + 0.3	V
	V_{OUT}	VOUT / SDA	V_{SS} - 0.3 to V_{DD} + 0.3	V
	V_{SDA}	VOUT / SDA	V_{SS} - 0.3 to V_{DD} + 0.3	V
	$V_{I/O}$	TEST1, TEST3	V_{SS} - 0.3 to V_{DD} + 0.3	V
		TEST2	V_{SS} - 0.3 to V_{SS} + 1.98	V
Junction temperature	T_j	-	-40 to +175	°C
Operation ambient temperature	T_{opr}	-	-40 to +125	°C
Storage temperature	T_{stg}	-	-40 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 5

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	TMSOP-8	Board A	-	160	-	°C/W
			Board B	-	133	-	°C/W
			Board C	-	-	-	°C/W
			Board D	-	-	-	°C/W
			Board E	-	-	-	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

1. Linear Hall effect sensor operation

1. 1 Power supply characteristics

Table 6

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V, V_{REF} = 2.5 V, S = 130 V/T, B = 0 mT, default value*1 unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	-	4.5	5.0	5.5	V	-
Current consumption	I_{DD}	Ta = -40°C to +125°C (T_j = -40°C to +150°C)	-	19	22	mA	1
UVLO release voltage	V_{UVLOR}	-	4.15	4.30	4.45	V	1
UVLO detection voltage	V_{UVLOD}	-	3.95	4.10	4.25	V	1
UVLO hysteresis voltage	$V_{UVLOHYS}$	-	-	0.2	-	V	-
UVLO detection delay time	t_{DELAY_UVLOD}	-	-	1.0	-	ms	-
Power-on reset threshold voltage	V_{PON}	-	-	2.90	-	V	-
Power-off threshold voltage	V_{POFF}	-	-	2.80	-	V	-
Power-on reset hysteresis voltage	V_{PHYS}	-	-	0.10	-	V	-
Thermal shutdown detection temperature	T_{SD}	Junction temperature	-	170	-	°C	-
Thermal shutdown release temperature	T_{SR}	Junction temperature	-	155	-	°C	-
Start up time	t_{PON}	C_{LOUT} = 4.7 nF, C_{LREF} = 47 nF	-	0.9	1.0	ms	-

***1.** The function settings and trimming adjustments of the IC are in the initial settings at the time of shipment.

1. 2 Magnetic characteristics

Table 7

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V, V_{REF} = 2.5 V, S = 130 V/T, B = 0 mT, default value*1 unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Maximum magnetic flux density*2	B_{MAX}	At minimum magnetic sensitivity setting		±350	-	-	mT	1
Sensitivity linearity error	LIN	Ta = -40°C to +125°C (T_j = -40°C to +150°C)		-0.5	-	0.5	%	1
Sensitivity	S	Initial settings at shipment		-	130	-	V/T	-
Sensitivity programming range	S_{RNG}	-		6	-	180	V/T	1
Sensitivity programming step	S_{STEP}	Formula A (S@n + 1 [LSB] - S@n [LSB]) / S@0 [LSB]		-	0.08	0.15	%	1
		Formula B (S@n + 1 [LSB] - S@n [LSB]) / S@n [LSB]		-	0.18	0.30	%	1
Sensitivity thermal drift	TCS	Ta = -40°C to +125°C (Tj = -40°C to +150°C)		-200	0	200	ppm/°C	1
Sensitivity thermal drift programming range	TCS_{RNG}	Ta = -40°C to +125°C (T_j = -40°C to +150°C)		-500	-	500	ppm/°C	1
Sensitivity thermal drift programming step	TCS_{STEP}	Ta = -40°C to +125°C (T_j = -40°C to +150°C)		-	25	-	ppm/°C	-
Output response time	t_{RSP_OUT}	C_{LOUT} = 4.7 nF, C_{LREF} = 47 nF, B = 10 mT, time from B 90% to V_{OUT} 90%	f_{BW} = 400 kHz	-	1.25	2.50	µs	1
			f_{BW} = 200 kHz	-	2.50	3.75	µs	1
			f_{BW} = 100 kHz	-	5.00	6.00	µs	1
Output reaction time	t_{RAC_OUT}	C_{LOUT} = 4.7 nF, C_{LREF} = 47 nF, B = 10 mT, time from B 10% to V_{OUT} 10%	f_{BW} = 400 kHz	-	0.75	1.75	µs	1
			f_{BW} = 200 kHz	-	1.25	2.00	µs	1
			f_{BW} = 100 kHz	-	2.00	3.00	µs	1
Output settling time*2	t_{SET_OUT}	C_{LOUT} = 4.7 nF, C_{LREF} = 47 nF, B = 10 mT, time from V_{OUT} 10% to stabilization within 3% of V_{OUT} steady status	f_{BW} = 400 kHz	-	2.5	5.0	µs	1
			f_{BW} = 200 kHz	-	4.0	6.5	µs	1
			f_{BW} = 100 kHz	-	5.5	8.0	µs	1
Output overshoot*2	OS	C_{LOUT} = 4.7 nF, C_{LREF} = 47 nF, B = 10 mT, overshoot against V_{OUT} steady status		-	-	10	%	1
Frequency bandwidth	f_{BW}	Initial settings at shipment, C_{LOUT} = 4.7 nF, C_{LREF} = 47 nF, frequency with a magnetic sensitivity of -3 dB		-	400	-	kHz	-
Frequency bandwidth programming range	f_{BWRNG}	C_{LOUT} = 4.7 nF, C_{LREF} = 47 nF, frequency with a magnetic sensitivity of -3 dB		-	400	-	kHz	-
				-	200	-	kHz	-
				-	100	-	kHz	-

***1.** The function settings and trimming adjustments of the IC are in the initial settings at the time of shipment.
***2.** This item is guaranteed by design.

Remark The unit of magnetic density mT can be converted by using the formula 1 mT = 10 Gauss.

1. 3 Output voltage characteristics

Table 8

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V, V_{REF} = 2.5 V, S = 130 V/T, B = 0 mT, default value*1 unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Output offset voltage	V_{OFF}	Initial settings at shipment		-	0	-	mV	1
Output offset voltage programming range	V_{OFFRNG}	-		-100	-	100	mV	1
Output offset voltage programming step	$V_{OFFSTEP}$	-		-	0.6	1.5	mV	1
Output offset voltage thermal drift	T_{CVOFF}	Ta = -40°C to +125°C (T_j = -40°C to +150°C)		-0.075	0	0.075	mV/°C	1
Output voltage "H"	V_{OUT_H}	Ta = -40°C to +125°C (T_j = -40°C to +150°C)		4.85	-	-	V	1
Output voltage "L"	V_{OUT_L}	Ta = -40°C to +125°C (T_j = -40°C to +150°C)		-	-	0.15	V	1
Output source current	I_{OUT_SOC}	V_{OUT} = V_{SS}		17	22	27	mA	2
Output sink current	I_{OUT_SNK}	V_{OUT} = V_{DD}		17	22	27	mA	2
Output resistance	R_{OUT}	I_{OUT} = ±1.25 mA, Ta = -40°C to +125°C (T_j = -40°C to +150°C)		-	1	4	Ω	3
Output pin load resistance	R_{LOUT}	Connected between the VOUT pin and the VSS pin, Ta = -40°C to +125°C (T_j = -40°C to +150°C)		2	-	-	kΩ	-
Output pin load capacitance	C_{LOUT}	Connected between the VOUT pin and the VSS pin, Ta = -40°C to +125°C (T_j = -40°C to +150°C)		0	4.7	6.0	nF	-
Input magnetic flux density referred noise voltage	B_{NOISE}	f = 10 kHz		-	0.09	-	$\mu T/\sqrt{Hz}$	-
Output noise voltage	V_{NOISE_RMS}	S = 30 V/T	f_{BW} = 400 kHz	-	1.89	-	mV_{rms}	-
			f_{BW} = 200 kHz	-	1.40	-	mV_{rms}	-
			f_{BW} = 100 kHz	-	1.08	-	mV_{rms}	-

***1.** The function settings and trimming adjustments of the IC are in the initial settings at the time of shipment.

1. 4 Reference voltage characteristics

Table 9

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V, V_{REF} = 2.5 V, S = 130 V/T, B = 0 mT, default value*1 unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Reference voltage output mode							
Reference voltage output	V_{REF}	Initial settings at shipment	2.48	2.50	2.52	V	1
Reference voltage programming range	V_{REFRNG}	V_{REF} = 2.50 V	-	2.50	-	V	1
		V_{REF} = 1.65 V	-	1.65	-	V	1
		V_{REF} = 1.50 V	-	1.50	-	V	1
		V_{REF} = 0.50 V	-	0.50	-	V	1
Reference voltage programming step	$V_{REFSTEP}$	V_{REF} = 2.50 V	-	2.5	4.0	mV	1
Reference voltage thermal drift	T_{CVREF}	V_{REF} = 2.5 V / 1.65 V / 1.5 V, Ta = -40°C to +125°C (Tj = -40°C to +150°C)	-100	0	100	ppm/°C	1
		V_{REF} = 0.5 V, Ta = -40°C to +125°C (Tj = -40°C to +150°C)	-150	0	150	ppm/°C	1
Reference voltage source current	I_{REF_SOC}	V_{REF} = V_{SS}	0.30	0.36	0.50	mA	4
Reference voltage sink current	I_{REF_SNK}	V_{REF} = V_{DD}	10.0	12.0	14.0	mA	4
Reference voltage output resistance	R_{REF}	I_{REF} = ±12.5 μA, Ta = -40°C to +125°C (T_j = -40°C to +150°C)	160	200	280	Ω	5
Reference voltage output pin load resistance	R_{LREF}	Connected between the VREF pin and the VSS pin, Ta = -40°C to +125°C (T_j = -40°C to +150°C)	200	-	-	kΩ	-
Reference voltage output pin load capacitance	C_{LREF}	Connected between the VREF pin and the VSS pin, Ta = -40°C to +125°C (T_j = -40°C to +150°C)	-	47	-	nF	-
Reference voltage input mode							
Reference voltage input	V_{REFIN}	-	0.50	-	2.65	V	5
Reference voltage input leakage current	I_{IN_REF}	V_{REF} = 0 V to 2.65 V	-	0.1	-	μA	-

***1.** The function settings and trimming adjustments of the IC are in the initial settings at the time of shipment.

2. Serial communication operations

2. 1 Pin capacitance

Table 10

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL pin input capacitance	C_{IN_SCL}	-	-	1	-	pF
SDA pin I/O capacitance	C_{I/O_SDA}	-	-	1	-	pF

2. 2 Memory characteristics

Table 11

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Endurance	N_W	-		1000	-	-	cycle / word*1
Data retention	-	365 days, 24 hours*2	T_j = +25°C	15	-	-	year
			T_j = +125°C	10	-	-	year
			T_j = +150°C	3	-	-	year
			T_j = +175°C	1	-	-	year

***1.** For each address (Word: 8-bit)

***2.** In the case where temperature changes occur over time, such as in a temperature cycle, this is the accumulated value of the time the IC is at high temperature.

2. 3 DC Electrical Characteristics

Table 12

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH_SCL}, V_{IH_SDA}	SCL pin*1, SDA pin	0.7 × V_{DD}	-	V_{DD} + 0.3	V
Low level input voltage	V_{IL_SCL}, V_{IL_SDA}	SCL pin, SDA pin	-0.3	-	0.3 × V_{DD}	V
Input leakage current	I_{IH_SCL}	SCL pin, V_{SCL} = V_{DD}	-	0.1	1.0	µA
	I_{IL_SCL}	SCL pin, V_{SCL} = V_{SS}	-	0.1	1.0	µA
	I_{IH_SDA}	SDA pin, V_{SDA} = V_{DD}	-	0.1	1.0	µA
Pull-up resistor*2	R_{PU_SDA}	SDA pin	320	380	460	Ω
Low level output current	I_{OL_SDA}	SDA pin, V_{SDA} = 0.6 V	8	12	-	mA

***1.** The voltage at the SCL pin is also used to disengage from the serial communication operation mode.

***2.** Current flows through the pull-up resistor during the period when the SDA pin is set to "L" during serial communication operation mode.

Note that this increases the amount of current consumed from the VDD pin by the current of $\frac{V_{DD}}{R_{PU\_SDA}}$ A in addition to the current consumption (I_{DD}) of the linear Hall effect sensor operation mode.

2. 4 AC Electrical Characteristics

2. 4. 1 Output load = 100 pF (SCL clock frequency ≤ 400 kHz)

Table 13 Measurement Conditions

Input pulse voltage	0.2 × V_{DD} to 0.8 × V_{DD}
Input pulse rising / falling time	20 ns or less
Output judgment voltage	0.3 × V_{DD} to 0.7 × V_{DD}
Output load	100 pF

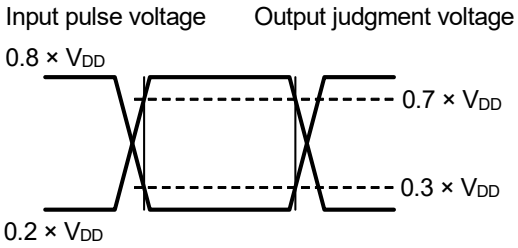


Figure 3 Input / Output Waveform during AC Measurement

Table 14

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	-	-	400	kHz
SCL clock time "L"	t_{LOW}	1300	-	-	ns
SCL clock time "H"	t_{HIGH}	600	-	-	ns
SCL, SDA rising time*1	t_R	-	-	300	ns
SCL, SDA falling time*1	t_F	-	-	300	ns
Data input setup time	$t_{SU.DAT}$	100	-	-	ns
Data input hold time	$t_{HD.DAT}$	0	-	-	ns
Data output delay time	t_{AA}	100	-	1100	ns
Data output hold time	t_{DH}	50	-	-	ns
Start condition setup time	$t_{SU.STA}$	600	-	-	ns
Start condition hold time	$t_{HD.STA}$	600	-	-	ns
Stop condition setup time	$t_{SU.STO}$	600	-	-	ns
Bus release time	t_{BUF}	13	-	-	ms
Noise suppression time	t_I	-	50	-	ns

***1.** This item is guaranteed by design.

2. 4. 2 Output load = 4.7 nF (SCL clock frequency ≤ 100 kHz)

Table 15 Measurement Conditions

Input pulse voltage	0.2 × V_{DD} to 0.8 × V_{DD}
Input pulse rising / falling time	1.0 µs or less
Output judgment voltage	0.3 × V_{DD} to 0.7 × V_{DD}
Output load	4.7 nF

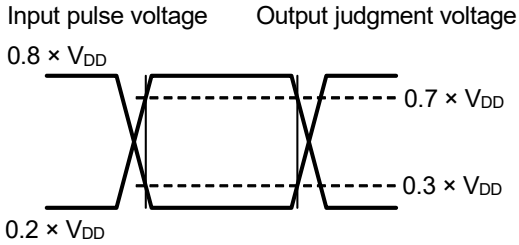


Figure 4 Input / Output Waveform during AC Measurement

Table 16

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	-	-	100	kHz
SCL clock time "L"	t_{LOW}	5.7	-	-	µs
SCL clock time "H"	t_{HIGH}	2.3	-	-	µs
SCL, SDA rising time*1	t_R	-	-	1.0	µs
SCL, SDA falling time*1	t_F	-	-	1.0	µs
Data input setup time	$t_{SU.DAT}$	0.25	-	-	µs
Data input hold time	$t_{HD.DAT}$	0	-	-	µs
Data output delay time	t_{AA}	0.1	-	5.45	µs
Data output hold time	t_{DH}	0.05	-	-	µs
Start condition setup time	$t_{SU.STA}$	4.0	-	-	µs
Start condition hold time	$t_{HD.STA}$	4.0	-	-	µs
Stop condition setup time	$t_{SU.STO}$	4.0	-	-	µs
Bus release time	t_{BUF}	13	-	-	ms
Noise suppression time	t_I	-	50	-	ns

***1.** This item is guaranteed by design.

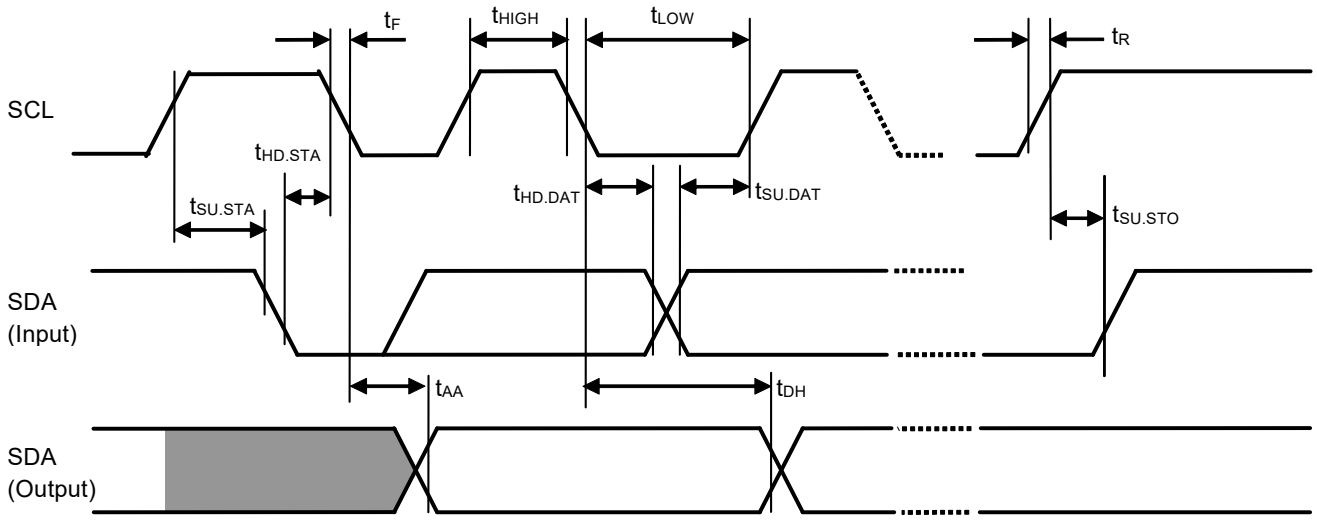


Figure 5 Bus Timing

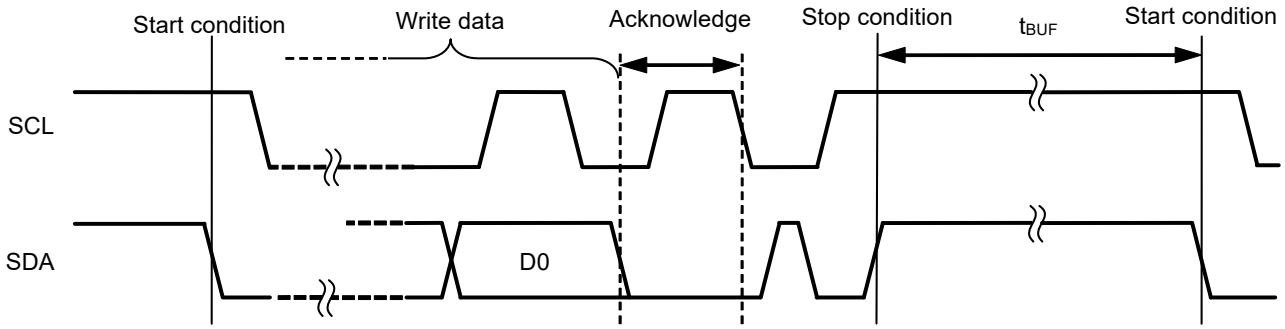


Figure 6 Write Cycle Timing

■ Test Circuits

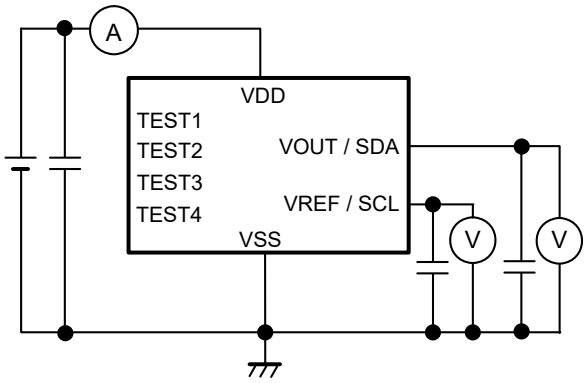


Figure 7 Test Circuit 1

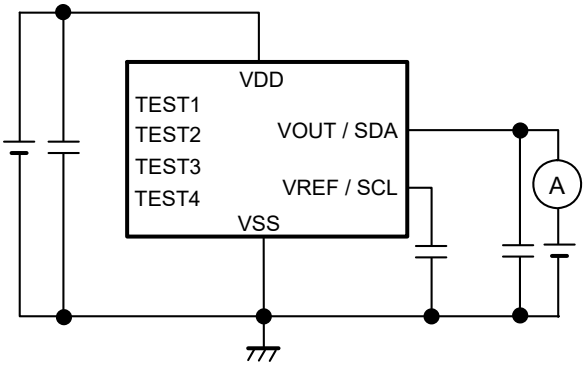


Figure 8 Test Circuit 2

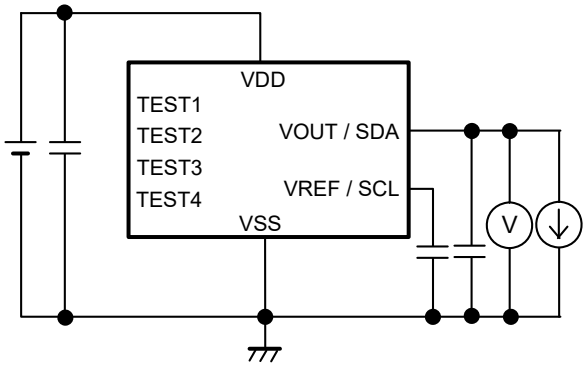


Figure 9 Test Circuit 3

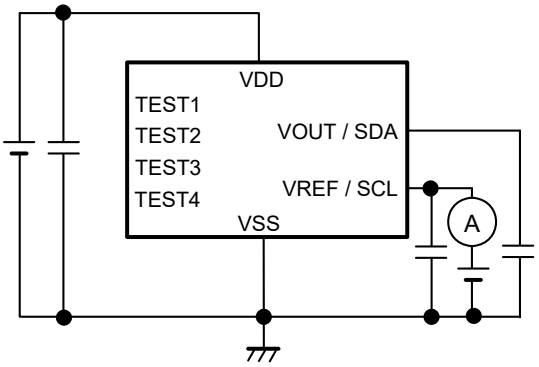


Figure 10 Test Circuit 4

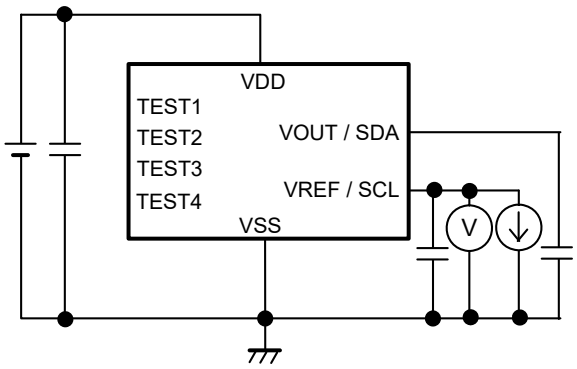


Figure 11 Test Circuit 5

■ Standard Circuits

1. Reference voltage output mode

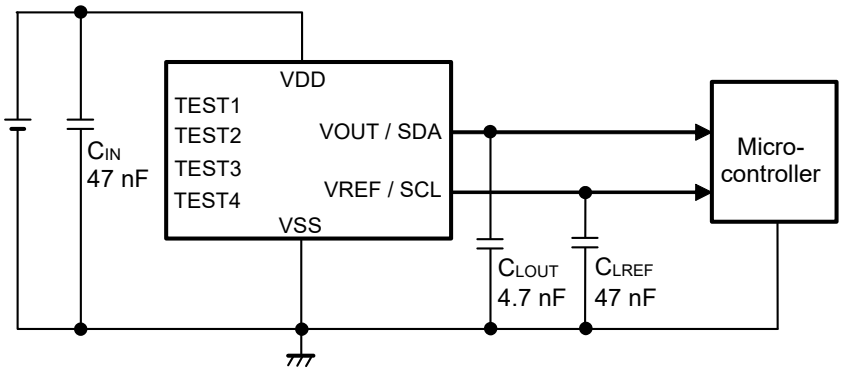


Figure 12 Standard Circuit (Reference Voltage Output Mode)

2. Reference voltage input mode

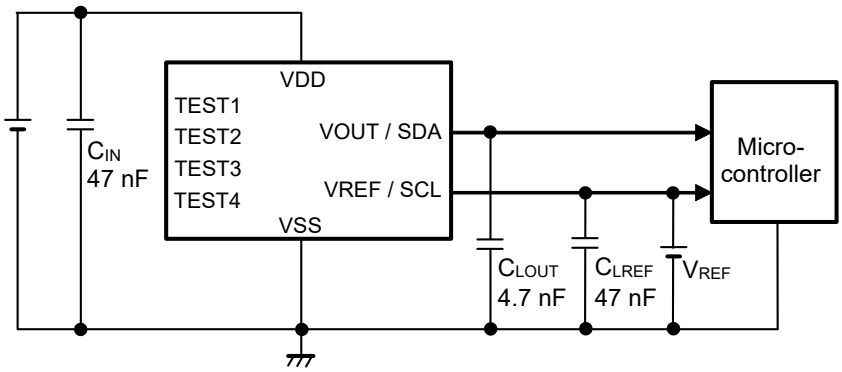


Figure 13 Standard Circuit (Reference Voltage Input Mode)

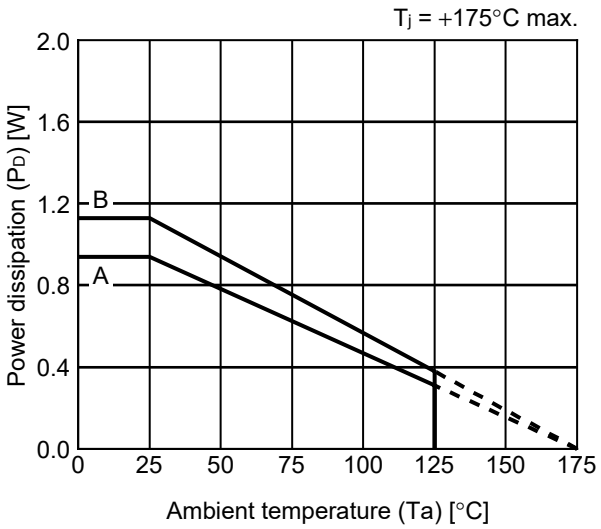
Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

■ Precautions

- Do not operate these ICs in excess of the absolute maximum ratings. Attention should be paid to the power supply voltage, especially. The surge voltage which exceeds the absolute maximum ratings can cause latch-up and malfunction. Perform operations after confirming the detailed operation condition in the data sheet.
- If the impedance of the power supply is high, the IC may malfunction due to a supply voltage drop caused by feed-through current. Take care with the pattern wiring to ensure that the impedance of the power supply is low.
- Note that the IC may malfunction if the power supply voltage rapidly changes. When the IC is used under the environment where the power supply voltage rapidly changes, it is recommended to judge the output voltage of the IC by reading it multiple times.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- The application conditions for the power supply voltage and the output resistor should not exceed the power dissipation.
- Large stress on this IC may affect the magnetic characteristics. Avoid large stress which is caused by the handling during or after mounting the IC on a board.
- Since the package heat radiation differs according to the conditions of the application, perform thorough evaluation with actual applications to confirm no problems occur.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Power Dissipation

TMSOP-8

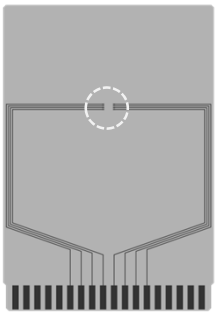


Board	Power Dissipation (P_D)
A	0.94 W
B	1.13 W
C	-
D	-
E	-

TMSOP-8 Test Board

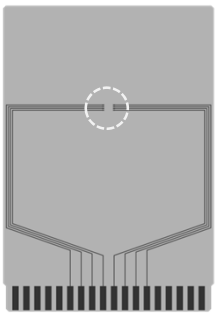
(1) Board A

IC Mount Area



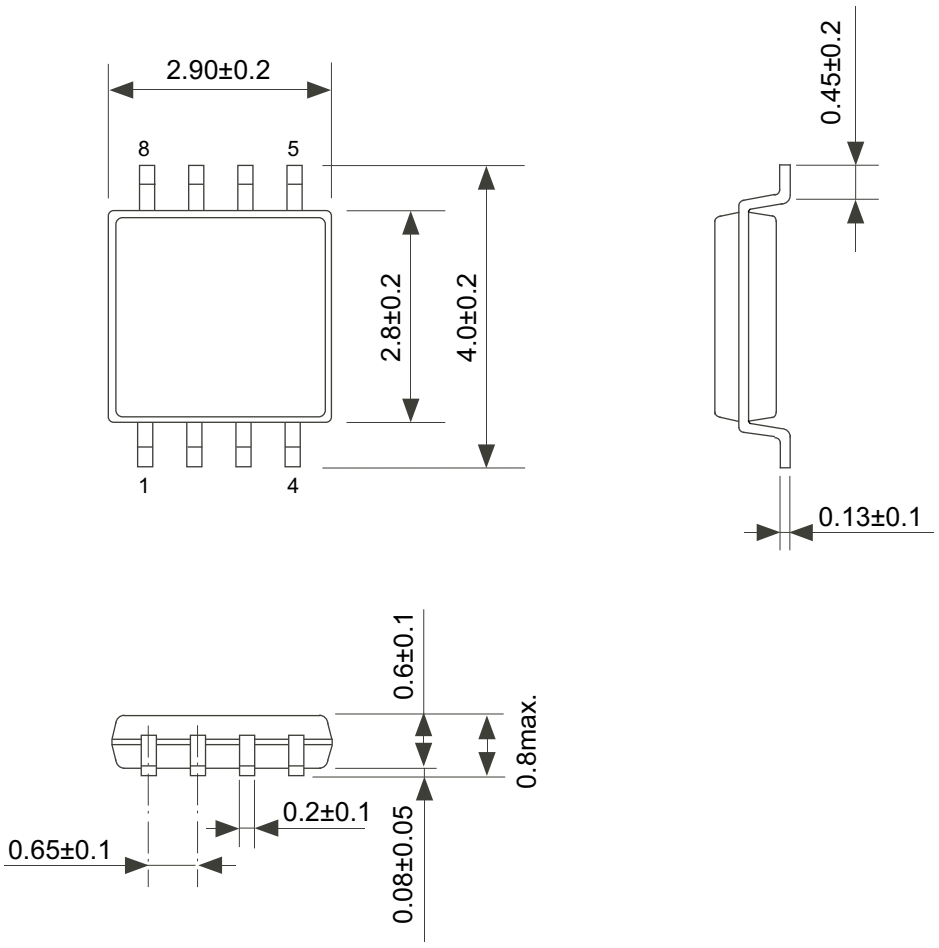
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

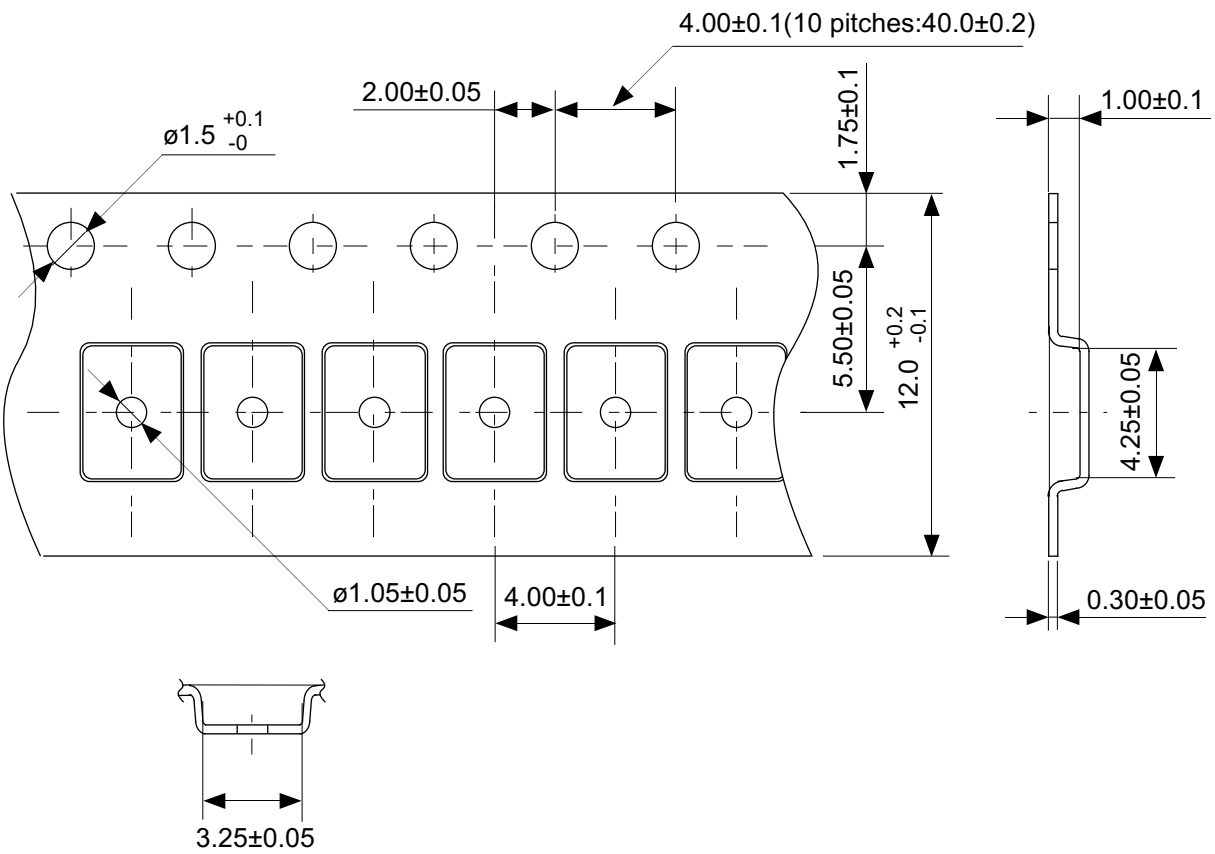
No. TMSOP8-A-Board-SD-1.0

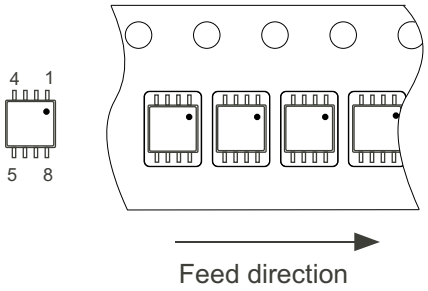


No. FM008-A-P-SD-1.2

TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.2
ANGLE	
UNIT	mm

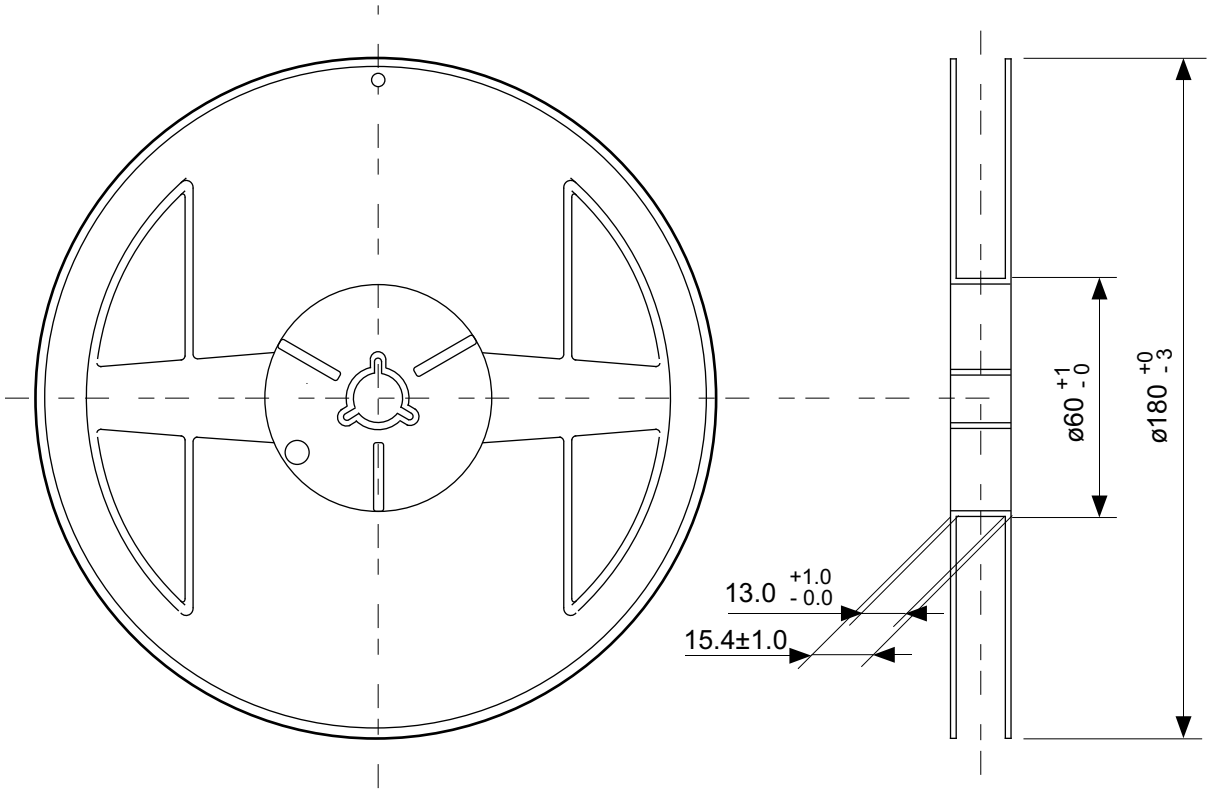
ABLIC Inc.



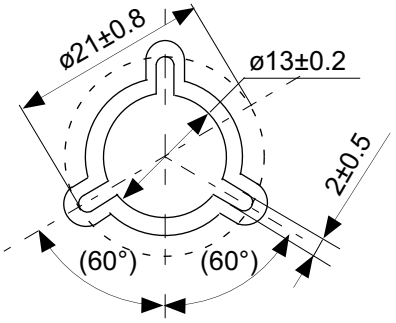


No. FM008-A-C-SD-3.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-3.0
ANGLE	
UNIT	mm
ABLIC Inc.	



Enlarged drawing in the central part



No. FM008-A-R-SD-2.0

TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-2.0		
ANGLE		QTY.	4,000
UNIT	mm		
	ABLIC Inc.		

Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the incorrect information described herein.
4. Be careful to use the products within their ranges described herein. Pay special attention for use to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by failures and / or accidents, etc. due to the use of the products outside their specified ranges.
5. Before using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc. The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party is strictly prohibited without the express permission of ABLIC Inc.
14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

2.4-2019.07