S-82K5A Series

BATTERY MONITORING IC FOR 3-SERIAL TO 5-SERIAL CELL PACK (SECONDARY PROTECTION)

www.ablic.com

Rev.1.0_00

This IC is used for secondary protection of lithium-ion rechargeable batteries, incorporating high-accuracy voltage detection circuits and delay circuits in a small 8-pin package.
Short-circuiting between cells makes it possible for serial connection of 3-cell to 5-cell.
By cascade connection of these ICs, it is possible to protect 6-serial or more cells lithium-ion rechargeable battery packs.

■ Features

- High-accuracy voltage detection circuit for each cell
  - Overcharge detection voltage n: 3.500 V to 4.700 V (5 mV steps) — Accuracy ±20 mV (Ta = +25°C), Accuracy ±25 mV (Ta = −10°C to +60°C)
  - Overcharge release voltage n*1: 3.100 V to 4.700 V — Accuracy ±50 mV
- Delay times for overcharge detection are generated only by an internal circuit (external capacitors are unnecessary)
  - Overcharge detection delay time: 0.5 s, 1 s, 2 s, 4 s, 6 s, 8 s
- CO pin output voltage is limited to 7.5 V max.
- Overcharge timer reset function: Available, unavailable
- High withstand voltage: Absolute maximum rating 28 V
- Wide operating voltage range: 3.6 V to 24 V
- Wide operating temperature range: Ta = −40°C to +85°C
- Low current consumption
  - During operation (3.4 V for each cell): 3.0 μA max.
- Lead-free (Sn 100%), halogen-free

***1.** Overcharge release voltage = Overcharge detection voltage - Overcharge hysteresis voltage
(Overcharge hysteresis voltage can be selected from a range of 0 mV to 400 mV in 50 mV step.)

Remark n = 1, 2, 3, 4, 5

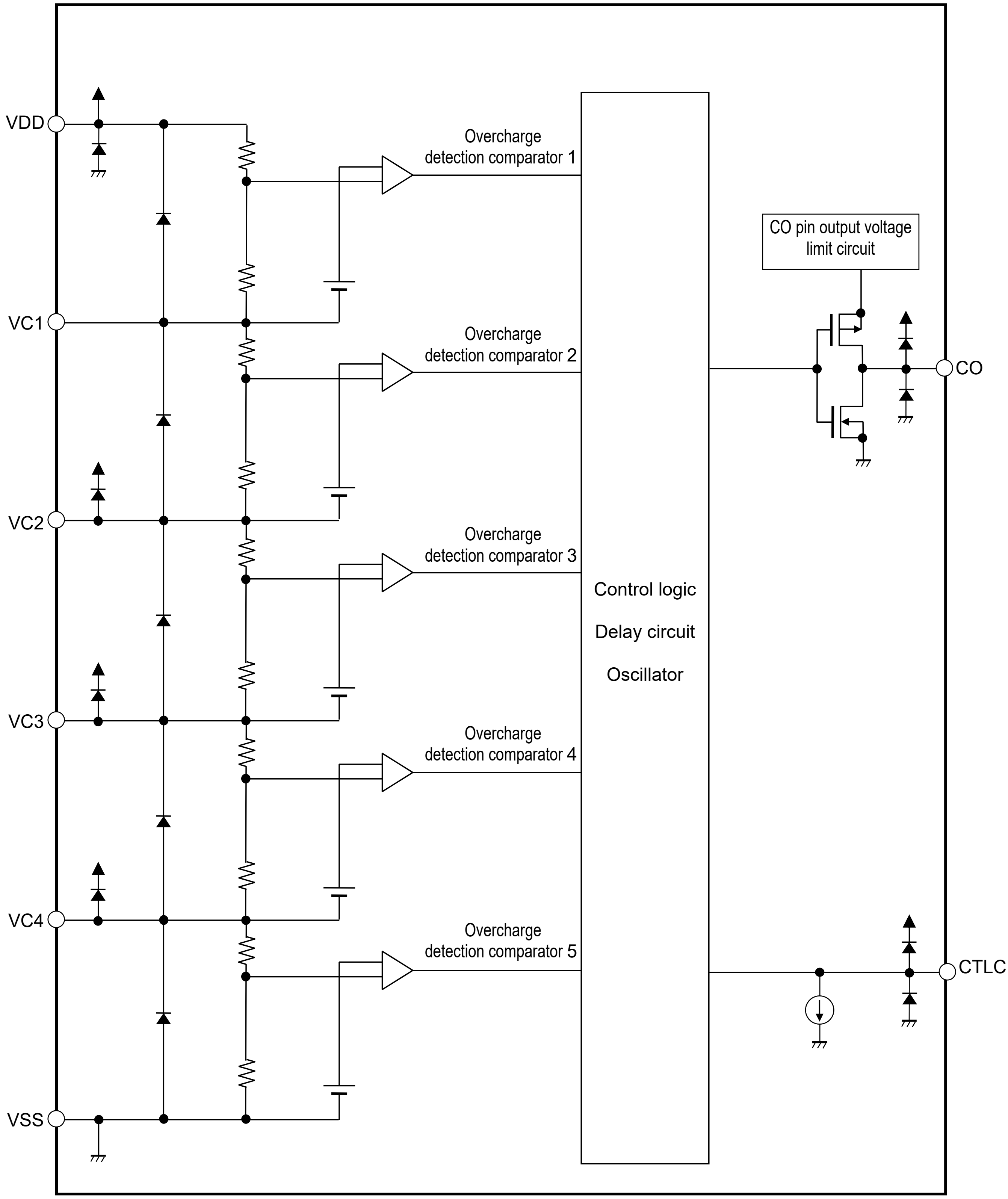
■ Applications

- Lithium-ion rechargeable battery pack

■ Packages

- TMSOP-8
- SNT-8A

■ Block Diagram



Remark Diodes in the figure are parasitic diodes.

Figure 1

■ Product Name Structure

1. Product name

S-82K5A xx - xxxx U

- U: Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- xxxx: Package abbreviation and IC packing specifications*1
  - K8T2: TMSOP-8, Tape
  - I8T1: SNT-8A, Tape
- xx: Serial code*2
  - Sequentially set from AA to ZZ

***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

2. Packages

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD	–
SNT-8A	PH008-A-P-SD	PH008-A-C-SD	PH008-A-R-SD	PH008-A-L-SD

3. Product name list

3. 1 TMSOP-8

Table 2

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Overcharge Detection Delay Time*1 [t_{CU}]	Overcharge Timer Reset function*2
S-82K5AAA-K8T2U	3.650 V	3.600 V	2.0 s	Unavailable

***1. Overcharge detection delay time:** 0.5 s, 1 s, 2 s, 4 s, 6 s, 8 s
***2. Overcharge timer reset function:** Available, unavailable

Remark Please contact our sales representatives for products other than the above.

■ Pin Configuration

1. TMSOP-8

Top view

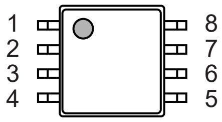


Figure 2

Table 3

Pin No.	Symbol	Description
1	VDD	Positive power supply input pin, Positive voltage connection pin of battery 1
2	VC1	Negative voltage connection pin of battery 1, Positive voltage connection pin of battery 2
3	VC2	Negative voltage connection pin of battery 2, Positive voltage connection pin of battery 3
4	VC3	Negative voltage connection pin of battery 3, Positive voltage connection pin of battery 4
5	VC4	Negative voltage connection pin of battery 4, Positive voltage connection pin of battery 5
6	VSS	Negative power supply input pin, Negative voltage connection pin of battery 5
7	CTLC	CO control pin
8	CO	Overcharge detection output pin

2. SNT-8A

Top view

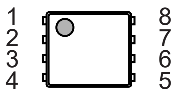


Figure 3

Table 4

Pin No.	Symbol	Description
1	VDD	Positive power supply input pin, Positive voltage connection pin of battery 1
2	VC1	Negative voltage connection pin of battery 1, Positive voltage connection pin of battery 2
3	VC2	Negative voltage connection pin of battery 2, Positive voltage connection pin of battery 3
4	VC3	Negative voltage connection pin of battery 3, Positive voltage connection pin of battery 4
5	VC4	Negative voltage connection pin of battery 4, Positive voltage connection pin of battery 5
6	VSS	Negative power supply input pin, Negative voltage connection pin of battery 5
7	CTLC	CO control pin
8	CO	Overcharge detection output pin

■ Absolute Maximum Ratings

Table 5

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin	V_{DS}	VDD	V_{SS} − 0.3 to V_{SS} + 28	V
Input pin voltage	V_{IN1}	VC1	V_{DD} − 6.0 to V_{DD} + 0.3, V_{IN2} − 0.3 to V_{IN2} + 6.0	V
	V_{IN2}	VC2	V_{IN3} − 0.3 to V_{IN3} + 6.0, V_{IN3} − 0.3 to V_{DD} + 0.3	V
	V_{IN3}	VC3	V_{IN4} − 0.3 to V_{IN4} + 6.0, V_{IN4} − 0.3 to V_{DD} + 0.3	V
	V_{IN4}	VC4	V_{SS} − 0.3 to V_{SS} + 6.0, V_{SS} − 0.3 to V_{DD} + 0.3	V
	V_{IN5}	CTLC	V_{SS} − 0.3 to V_{SS} + 28	V
Output pin voltage	V_{OUT}	CO	V_{SS} − 0.3 to V_{DD} + 0.3	V
Operation ambient temperature	T_{opr}	−	−40 to +85	°C
Storage temperature	T_{stg}	−	−40 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance

Table 6

Items	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	TMSOP-8	Board A	−	160	−	°C/W
			Board B	−	133	−	°C/W
			Board C	−	−	−	°C/W
			Board D	−	−	−	°C/W
			Board E	−	−	−	°C/W
		SNT-8A	Board A	−	211	−	°C/W
			Board B	−	173	−	°C/W
			Board C	−	−	−	°C/W
			Board D	−	−	−	°C/W
			Board E	−	−	−	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "**■ Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

Table 7

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage n (n = 1, 2, 3, 4, 5)	V_{CUn}	V1 = V2 = V3 = V4 = V5 = V_{CU} – 0.1 V	V_{CU} – 0.020	V_{CU}	V_{CU} + 0.020	V	1
		Ta = –10°C to +60°C*1, V1 = V2 = V3 = V4 = V5 = V_{CU} – 0.1 V	V_{CU} – 0.025	V_{CU}	V_{CU} + 0.025	V	1
Overcharge release voltage n (n = 1, 2, 3, 4, 5)	V_{CLn}	–	V_{CL} – 0.050	V_{CL}	V_{CL} + 0.050	V	2
Input voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP}	–	3.6	–	24	V	–
Output Voltage							
CO pin voltage "H"	V_{COH}	–	5.0	6.0	7.5	V	2
Input Current							
Current consumption during operation	I_{OPE}	V1 = V2 = V3 = V4 = V5 = 3.4 V, SW1 ON, SW2 OFF, SW3 OFF, SW4 OFF, SW5 OFF	–	1.0	3.0	μA	2
VCn pin current (n = 1, 2, 3, 4)	I_{VCn}	V1 = V2 = V3 = V4 = V5 = 3.4 V, SW1 ON, SW2 OFF, SW3 OFF, SW4 OFF, SW5 OFF	–0.6	0	0.6	μA	2
Output current							
CO pin sink current	I_{COL}	–	20	–	–	μA	2
CO pin source current	I_{COH}	–	–	–	–20	μA	2
Delay Time							
Overcharge detection delay time	t_{CU}	–	t_{CU} × 0.7	t_{CU}	t_{CU} × 1.3	–	2
Overcharge timer reset delay time	t_{TR}	–	6	12	20	ms	2
Control Pin							
CTLC pin reverse voltage	V_{CTLC}	–	0.2	0.7	2.0	V	2
CTLC pin reverse voltage during communication	V_{CTLC_C}	5.1 MΩ resistor connected to the CTLC pin	V_{DS} + 0.2	V_{DS} + 1.2	V_{DS} + 2.5	V	2
CTLC pin curent "H"	I_{CTLCH}	–	–	0.1	0.3	μA	2
CTLC pin curent "L"	I_{CTLCL}	–	–0.1	0.0	0.1	μA	2

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

■ Test Circuits

In the initial status of the test circuit, SW2, SW3, SW4, and SW5 should be OFF.

1. Overcharge detection voltage n (V_{CUn}) (Test circuit 1)

After setting V1 = V2 = V3 = V4 = V5 = V_{CU} − 0.1 V, V1 is gradually increased. When the CO pin output inverts, the voltage V1 is defined as the overcharge detection voltage 1 (V_{CU1}). Other overcharge detection voltage n (V_{CUn}) can be determined in the same way as when n = 1.

2. Overcharge release voltage n (V_{CLn}) (Test circuit 2)

Set SW1 to ON, V1 = V_{CU} + 0.1 V, and V2 = V3 = V4 = V5 = V_{CL} − 0.1 V to invert the CO pin output. After that, V1 is gradually decreased. When the CO pin output inverts again, the voltage V1 is defined as the overcharge release voltage (V_{CL1}). Other overcharge release voltage n (V_{CLn}) can be determined in the same way as when n = 1.

Remark n = 1, 2, 3, 4, 5

3. CO pin output voltage "H" (V_{COH}) (Test circuit 2)

The CO pin output voltage "H" (V_{COH}) is the voltage between the CO pin and the VSS pin when setting SW1 to ON, V1 = 4.8 V, V2 = V3 = V4 = V5 = 3.05 V, I1 = 0.1 μA, and SW5 to ON.

4. CO pin source current (I_{COH}), CO pin sink current (I_{COL}) (Test circuit 2)

Set SW4 to ON after setting SW1 to ON, V1 = 4.8 V, V2 = V3 = V4 = V5 = 3.05 V, and V7 = V_{COH} − 0.5 V. The CO pin current is the CO pin source current (I_{COH}) at that time.
Set SW4 to ON after setting SW1 to ON, V1 = V2 = V3 = V4 = V5 = 3.4 V, and V7 = 0.5 V. The CO pin current is the CO pin sink current (I_{COL}) at that time.

5. Overcharge detection delay time (t_{CU}) (Test circuit 2)

After setting SW1 to ON, V5 = V_{CU} − 0.2 V, and V1 = V2 = V3 = V4 = 3.4 V, V5 is increased to V_{CU} + 0.2 V. The overcharge detection delay time (t_{CU}) is the time period until the CO pin output inverts.

6. CTLC pin reverse voltage (V_{CTLC}) (Test circuit 2)

Set SW2 to ON after setting SW1 to OFF, V1 = V2 = V3 = V4 = V5 = 3.4 V, and V6 = 17 V. When the voltage V6 is gradually decreased and the CO pin output inverts, V6 is defined as the CTLC pin reverse voltage (V_{CTLC}).

7. CTLC pin reverse voltage during communication (V_{CTLC_C}) (Test circuit 2)

Set SW3 to ON after setting SW1 to OFF, V1 = V2 = V3 = V4 = V5 = 3.4 V, and V6 = 17 V. When the voltage V6 is gradually increased and the CO pin output inverts, V6 is defined as the CTLC pin reverse voltage during communication (V_{CTLC_C}).

8. Current consumption during operation (I_{OPE}) (Test circuit 2)

Set SW1 to ON and V1 = V2 = V3 = V4 = V5 = 3.4 V. The current consumption during operation (I_{OPE}) is I_{VDD} at that time.

9. Overcharge timer reset delay time (t_{TR}) (Test circuit 2)

Increase V1 up to 5.0 V (first rise) after setting SW1 to ON and V1 = V2 = V3 = V4 = V5 = 3.4 V, and decrease V1 down to 3.4 V within t_{CU}. After that, increase V1 up to 5.0 V again (second rise), and detect the time period till the CO pin output changes.
When the period from when V1 has fallen to the second rise is short, CO pin output changes after t_{CU} has elapsed since the first rise. If the period is gradually made longer, CO pin output changes after t_{CU} has elapsed since the second rise. The overcharge timer reset delay time (t_{TR}) is the period from V1 fall till the second rise at that time.

10. CTLC pin current "H" (I_{CTLCH}), CTLC pin current "L" (I_{CTLCL}) (Test circuit 2)

Set SW1 to OFF, SW2 to ON, V1 = V2 = V3 = V4 = V5 = 3.4 V, and V6 = 17 V. The CTCL pin current is the CTLC pin current "H" (I_{CTLCH}) at that time.
Set SW1 to OFF, SW2 to ON, V1 = V2 = V3 = V4 = V5 = 3.4 V, and V6 = 0 V. The CTLC pin current is the CTLC pin current "L" (I_{CTLCL}) at that time.

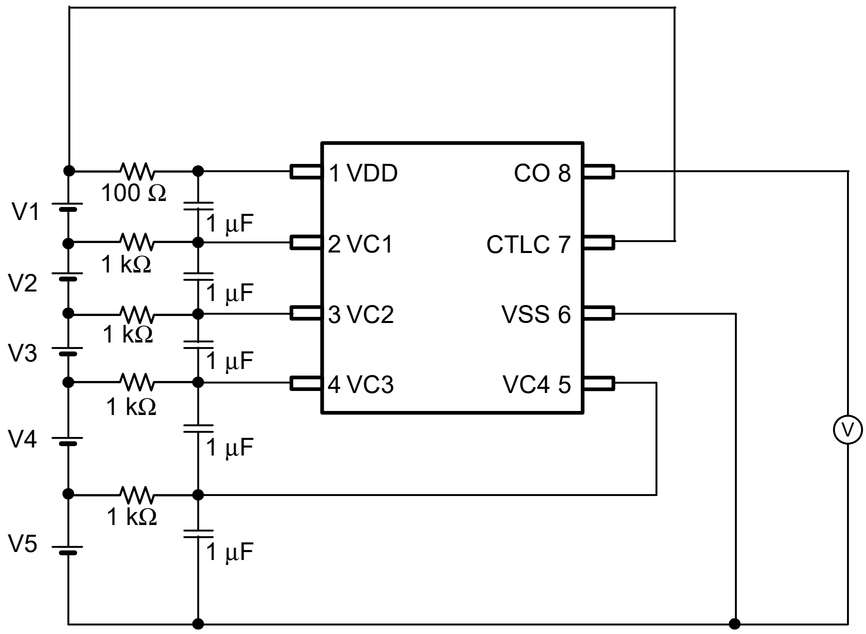


Figure 4 Test Circuit 1

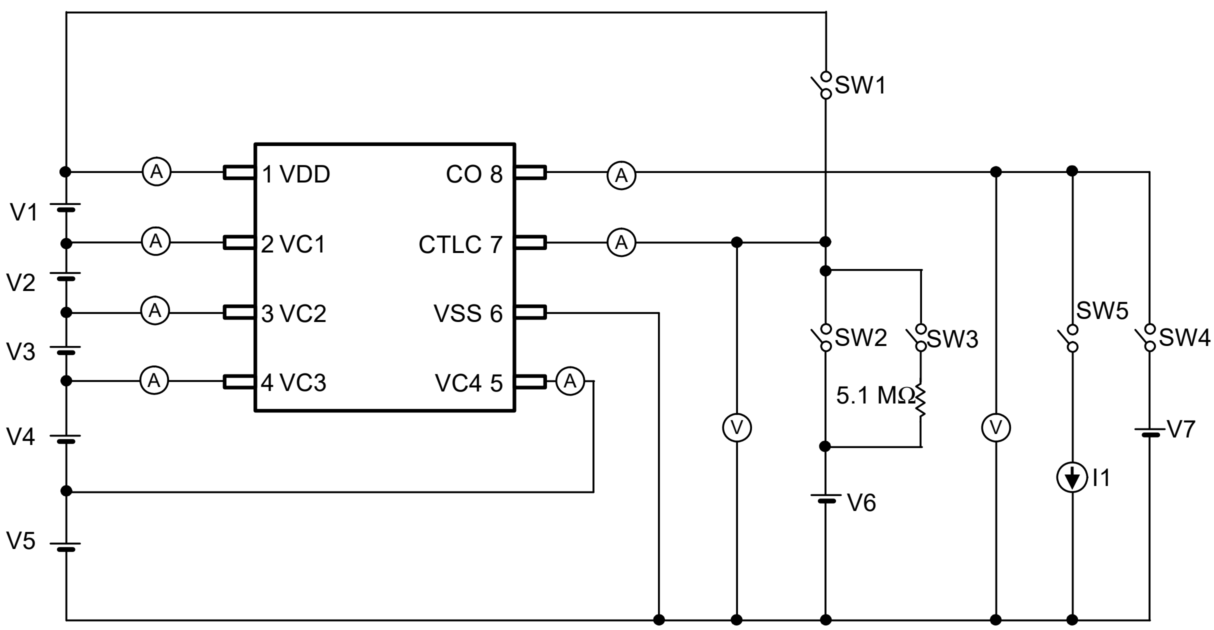


Figure 5 Test Circuit 2

■ Operation

1. Normal status

When the voltage of all batteries is less than or equal to the overcharge detection voltage n (V_{CUn}), the CO pin outputs "L". This status is called the normal status.

2. Overcharge status

When the voltage of any of the batteries exceeds the overcharge detection voltage n (V_{CUn}) during charging and this condition continues for the overcharge detection delay time (t_{CU}) or longer, the CO pin output inverts. This status is called the overcharge status.
When the voltage of all batteries falls below the overcharge release voltage n (V_{CLn}), the overcharge status is released, and this IC returns to its normal status.

3. Overcharge timer reset function

During t_{CU}, which is from when the voltage of any of the batteries being charged exceeds V_{CUn} until charging stops, this IC has the following operations.
Even if an overcharge release noise, which temporarily forces the battery voltage below V_{CUn}, is input, t_{CU} is continuously counted as long as the overcharge release noise time is shorter than the overcharge timer reset delay time (t_{TR}). Under the same conditions, if the overcharge release noise time is t_{TR} or longer, counting of t_{CU} is reset once. After that, when V_{CUn} has been exceeded, counting of t_{CU} resumes.

Remark n = 1, 2, 3, 4, 5

4. CTLC pin

The CTLC pin controls the CO pin. These controls precede the battery protection circuit.

Table 8 Status Set by CTLC Pin

CTLC Pin	CO pin
V_{SS} level ≤ CTLC pin voltage < V_{CTLC}	"H"
V_{CTLC} ≤ CTLC pin voltage < V_{DD} level	"L"
V_{DD} level ≤ CTLC pin voltage < V_{CTLC_C}	"L"
V_{CTLC_C} ≤ CTLC pin voltage	"H"

Remark The CTLC pin is at the V_{DD} level or higher in cascade connection. Connect a resistor of 5.1 MΩ to the CTLC pin in this case.
V_{CTLC}: CTLC pin reverse voltage
V_{CTLC_C}: CTLC pin reverse voltage during communication

■ Timing Charts

1. Overcharge detection operation (With overcharge timer reset function)

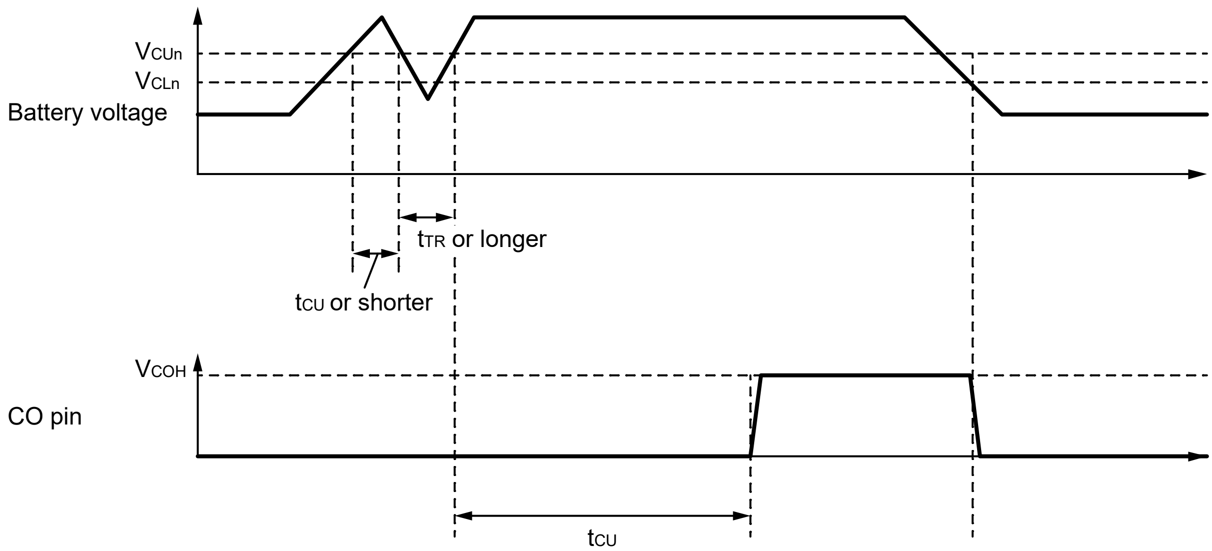


Figure 6

2. Overcharge timer reset operation (With overcharge timer reset function)

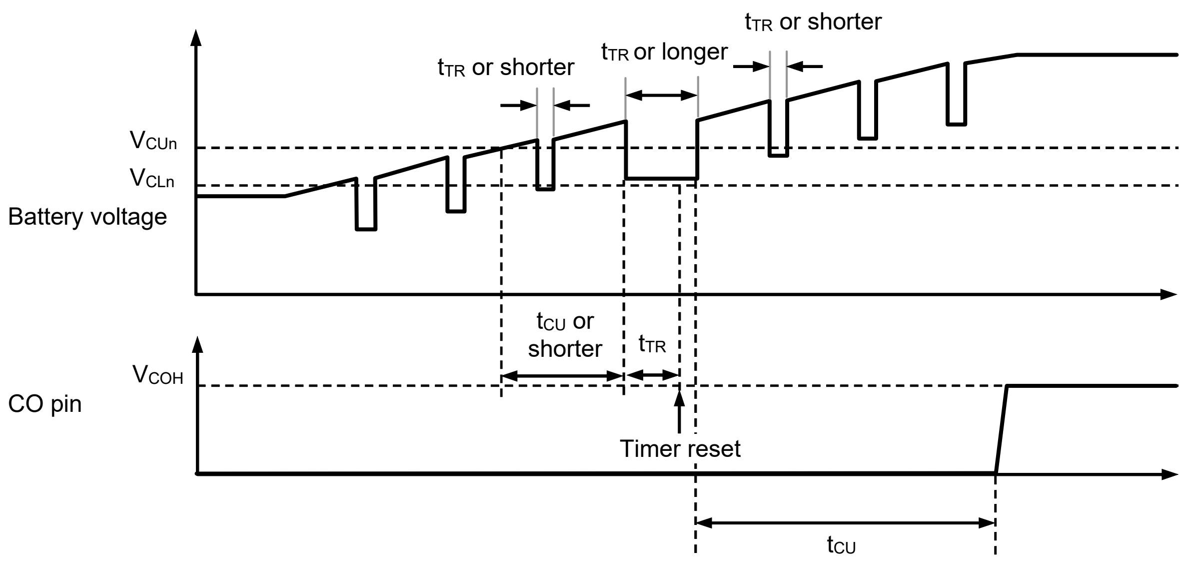
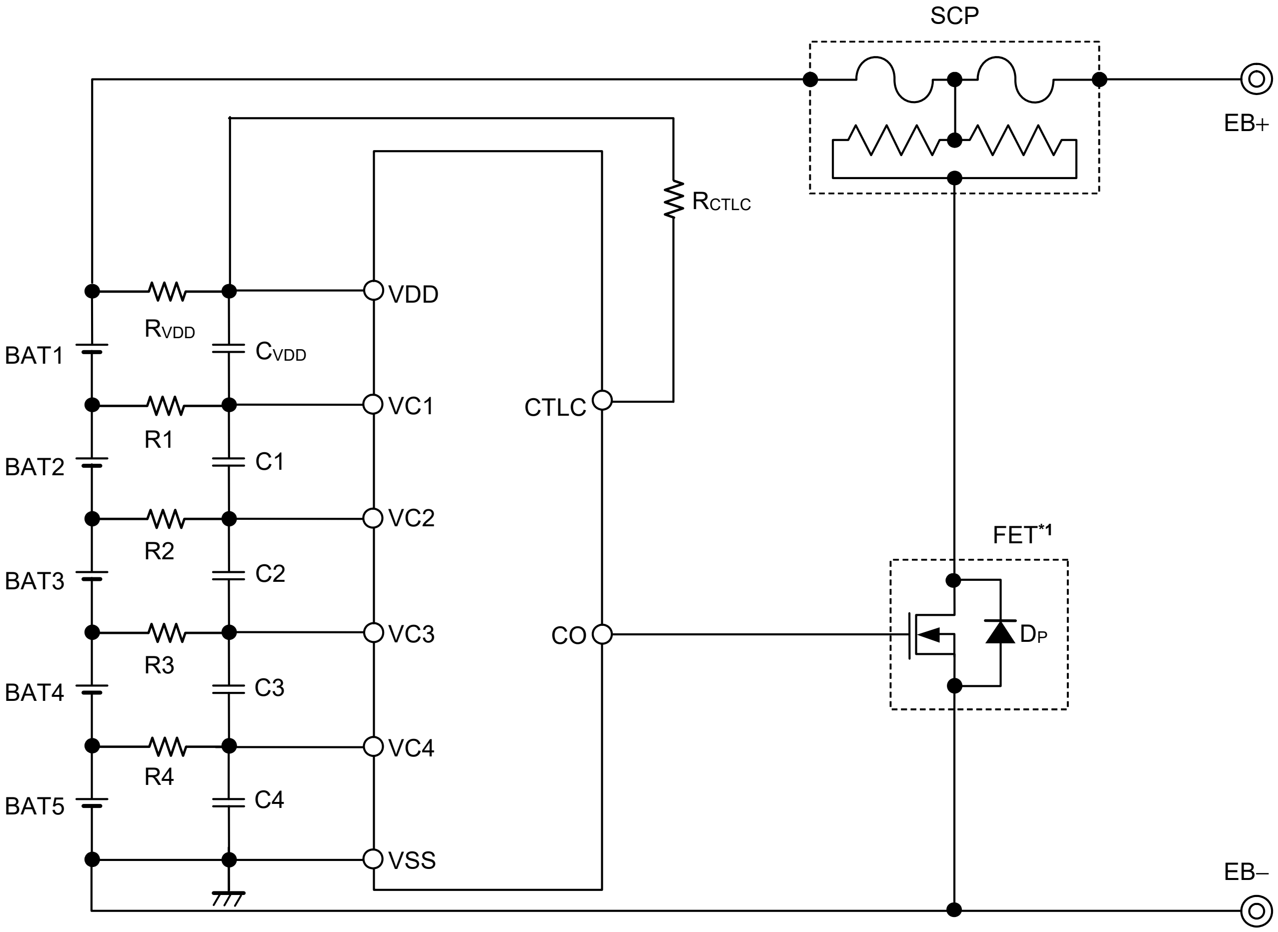


Figure 7

Remark n = 1, 2, 3, 4, 5

■ Connection Examples of Battery Monitoring IC

1. 5-serial cell



***1.** This IC limits its CO pin output voltage to 7.5 V max., so a FET with the gate withstand voltage of 8 V can be used.

Figure 8

Table 9 Constants for External Components

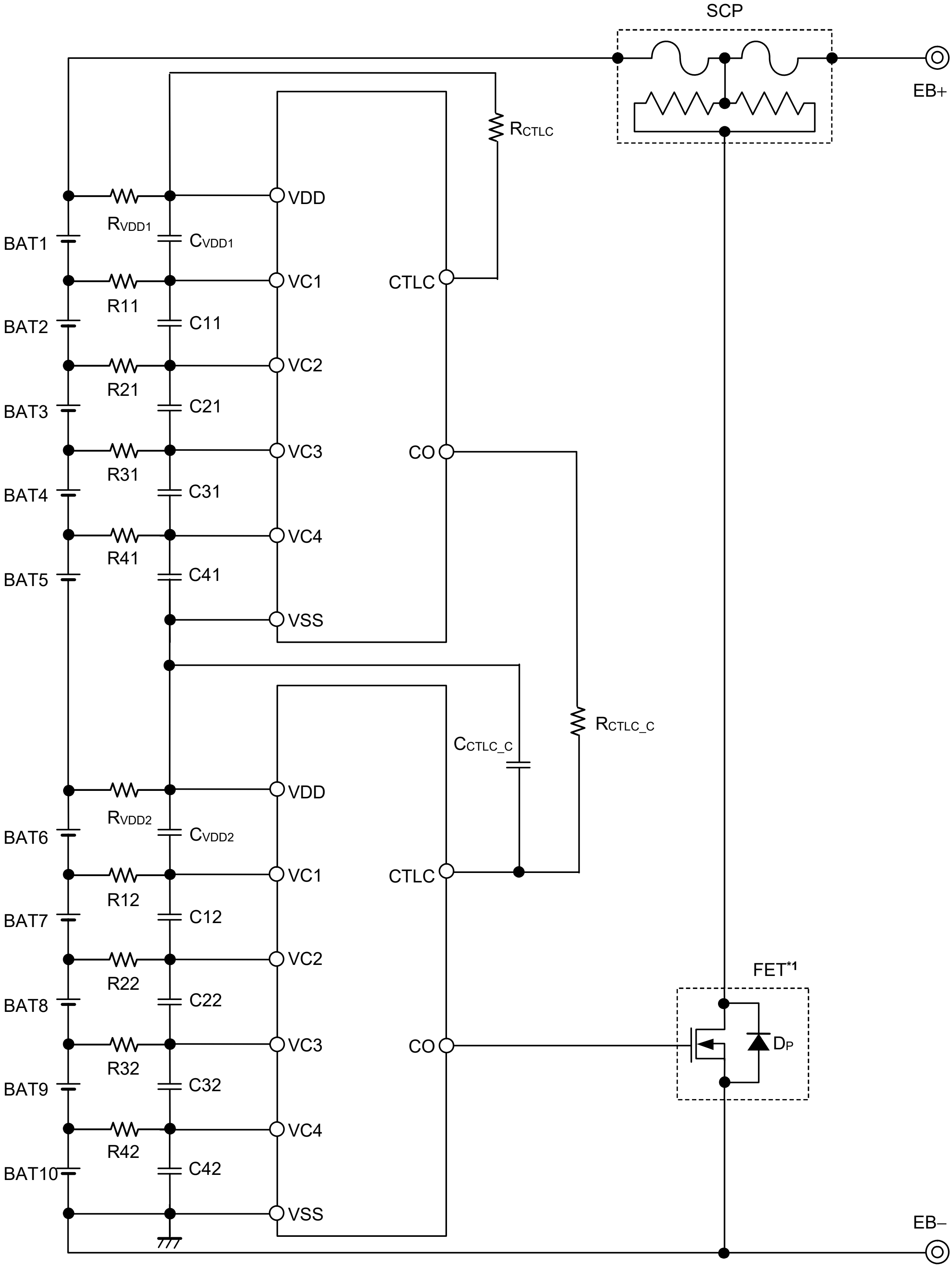
No.	Part	Typ.	Unit
1	R1 to R4	1	kΩ
2	C1 to C4, C_{VDD}	1	μF
3	R_{VDD}	100	Ω
4	R_{CTLC}	1	kΩ

Caution 1. The constants may be changed without notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using an actual application to set the constants.

3. Since the CO pin may become the detection status transiently when the battery is being connected, connect the positive terminal of BAT1 last in order to prevent the protection fuse from cutoff.

2. 10-serial cell

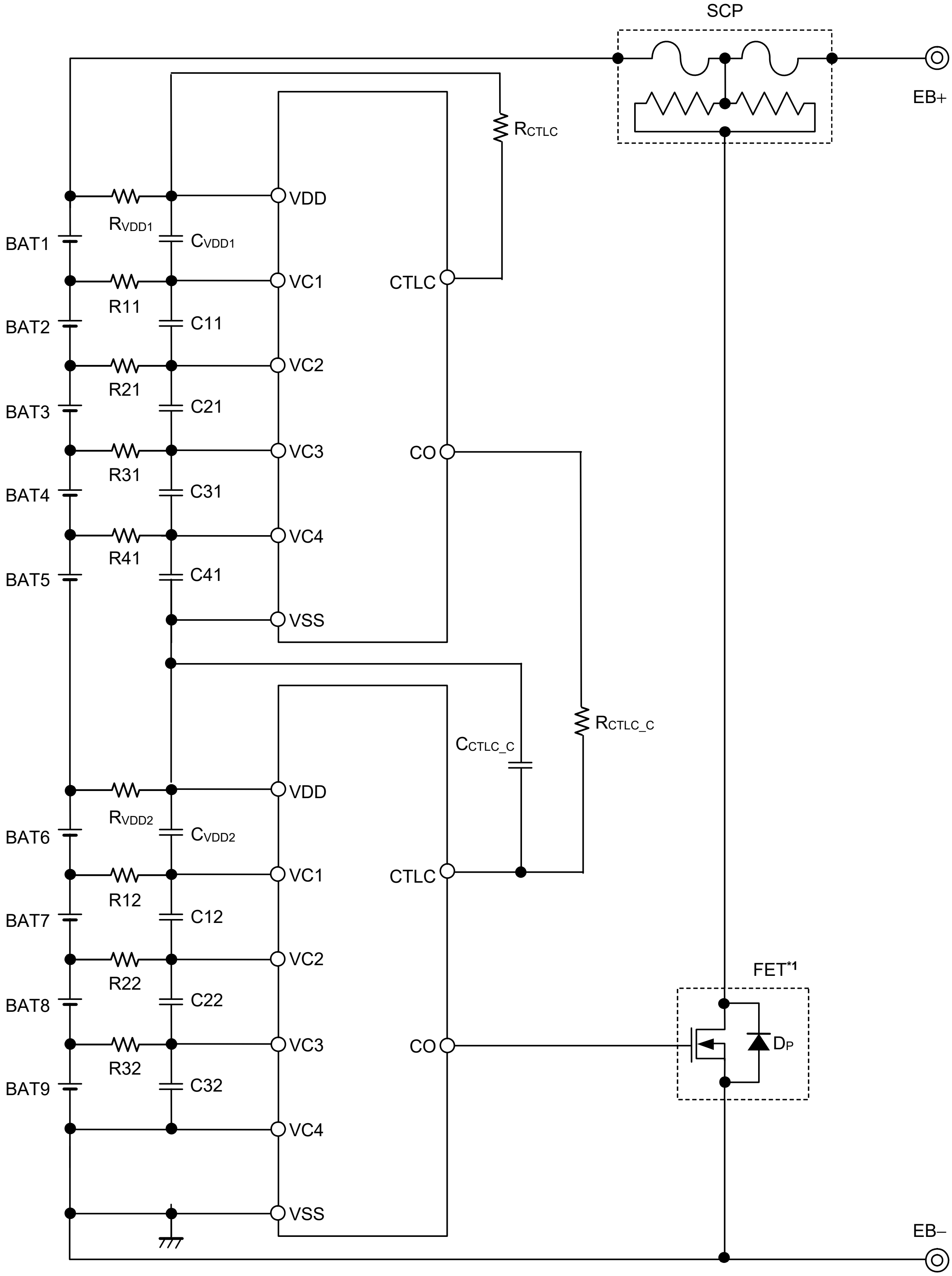


***1.** This IC limits its CO pin output voltage to 7.5 V max., so a FET with the gate withstand voltage of 8 V can be used.

Figure 9

Remark Regarding the recommended values for external components, refer to "**Table 10 Constants for External Components**".

3. 9-serial cell

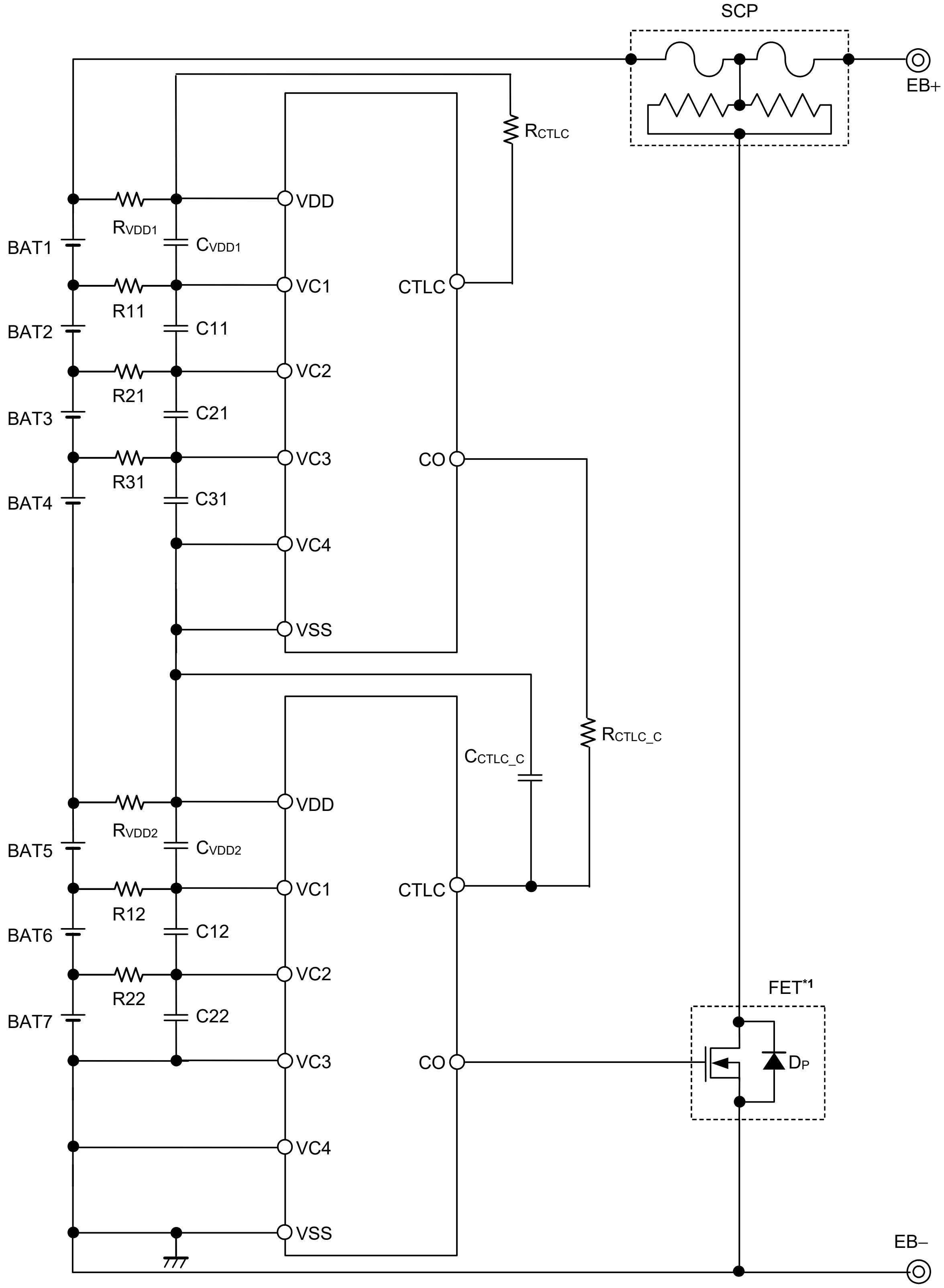


***1.** This IC limits its CO pin output voltage to 7.5 V max., so a FET with the gate withstand voltage of 8 V can be used.

Figure 10

Remark Regarding the recommended values for external components, refer to "**Table 10 Constants for External Components**".

4. 7-serial cell



***1.** This IC limits its CO pin output voltage to 7.5 V max., so a FET with the gate withstand voltage of 8 V can be used.

Figure 11

Remark Regarding the recommended values for external components, refer to "**Table 10 Constants for External Components**".

Table 10 Constants for External Components

No.	Part	Typ.	Unit
1	R11 to R41, R12 to R42	1	kΩ
2	C11 to C41, C12 to C42, C_{VDD1}, C_{VDD2}	1	μF
3	R_{VDD1}, R_{VDD2}	100	Ω
4	R_{CTLC}	1	kΩ
5	R_{CTLC_C}	5.1	MΩ
6	C_{CTLC_C}	0.01	μF

Caution 1. The constants may be changed without notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using an actual application to set the constants.

3. Since the CO pin may become the detection status transiently when the battery is being connected, connect the positive terminal of BAT1 last in order to prevent the protection fuse from cutoff.

[For SCP, contact]

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Kyobashi, Chuo-ku, Tokyo 104-0031, Japan
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https://www.dexerials.jp/en/

Precautions

- Do not connect batteries charged with V_{CL} or higher.

- If the connected batteries include a battery charged with V_{CL} or higher, this IC may become the overcharge status after all pins are connected.

- In some application circuits, even if an overcharged battery is not included, the order of connecting batteries may be restricted to prevent transient output of the CO pin detection pulses when the batteries are connected. Perform thorough evaluation with the actual application circuit.

- The application conditions for the input voltage, the output voltage, and the load current should not exceed the power dissipation.

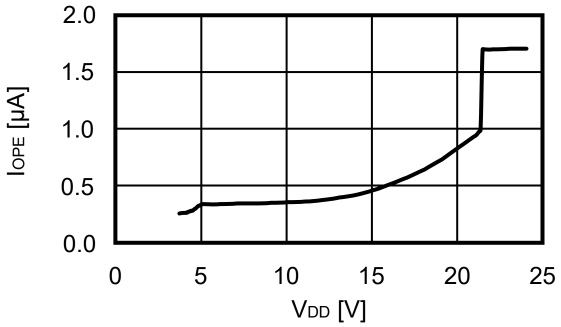
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

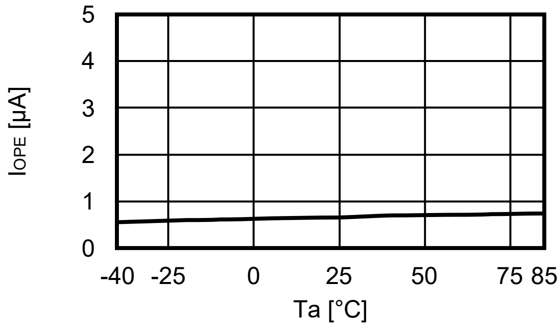
■ Characteristics (Typical Data)

1. Current consumption

1. 1 I_{OPE} vs. V_{DD}

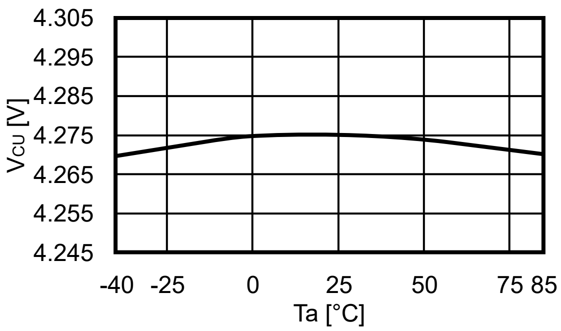


1. 2 I_{OPE} vs. Ta

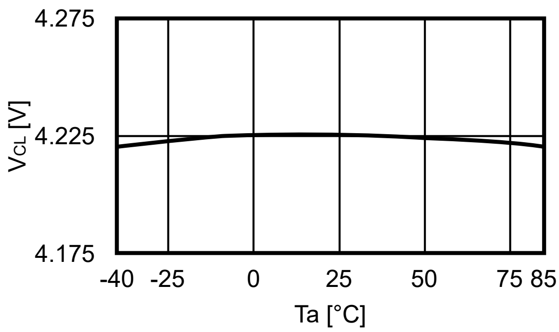


2. Detection voltage, release voltage

2. 1 V_{CU} vs. Ta

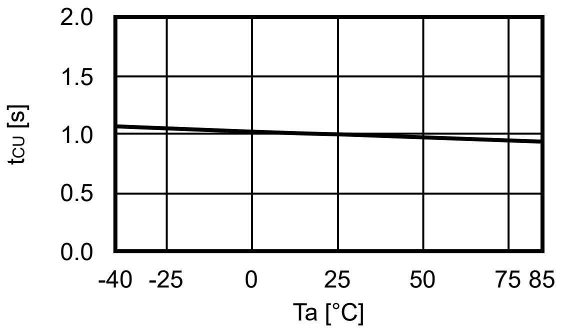


2. 2 V_{CL} vs. Ta



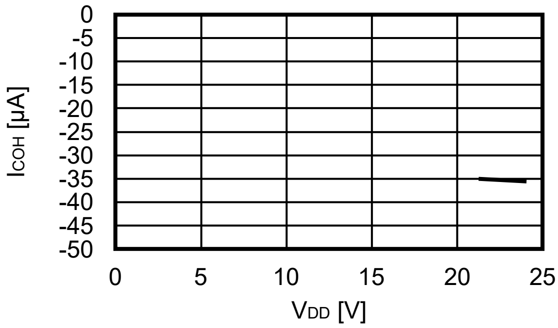
3. Delay time

3. 1 t_{CU} vs. Ta

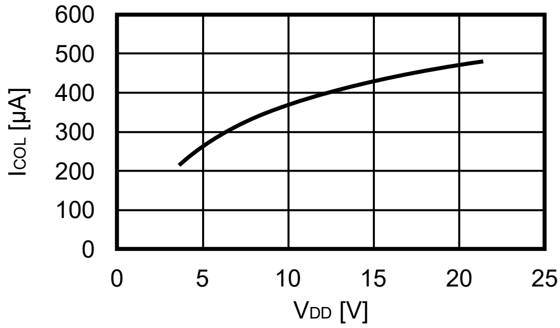


4. Output pin

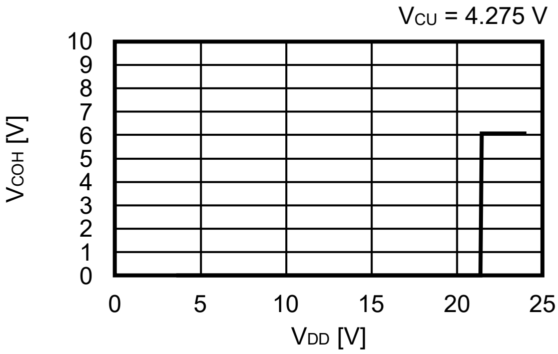
4. 1 I_{COH} vs. V_{DD}



4. 2 I_{COL} vs. V_{DD}

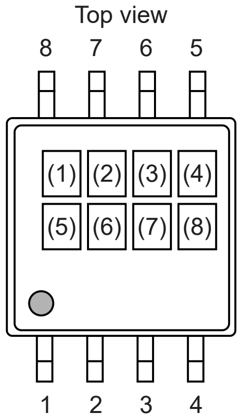


4. 3 V_{COH} vs. V_{DD}



■ Marking Specifications

1. TMSOP-8

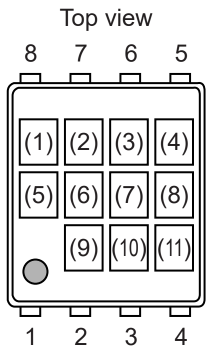


(1): Blank
(2) to (4): Product code (refer to **Product name vs. Product code**)
(5): Blank
(6) to (8): Lot number

Product name vs. Product code

Product Name	Product Code		
	(2)	(3)	(4)
S-82K5AAA-K8T2U	b	F	B

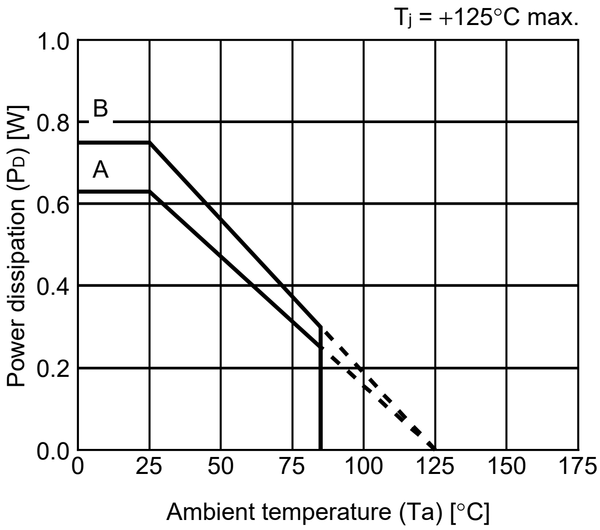
2. SNT-8A



(1): Blank
(2) to (4): Product code
(5), (6): Blank
(7) to (11): Lot number

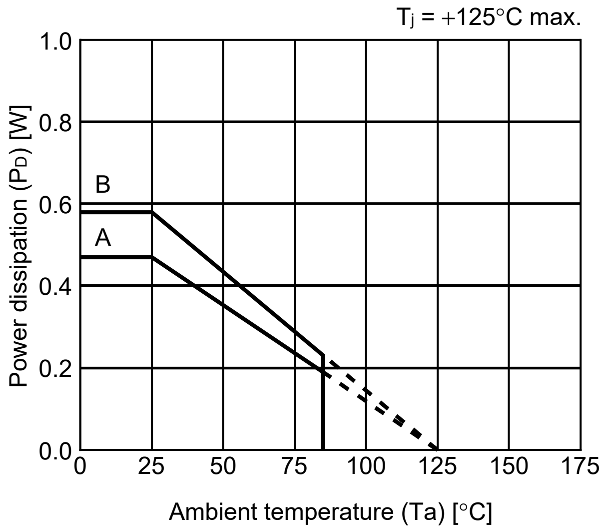
■ Power Dissipation

TMSOP-8



Board	Power Dissipation (PD)
A	0.63 W
B	0.75 W
C	–
D	–
E	–

SNT-8A

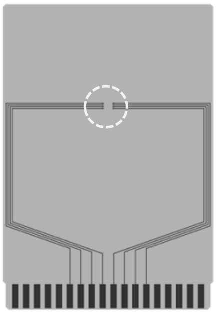


Board	Power Dissipation (PD)
A	0.47 W
B	0.58 W
C	–
D	–
E	–

TMSOP-8 Test Board

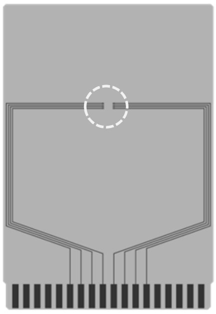
IC Mount Area

(1) Board A



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



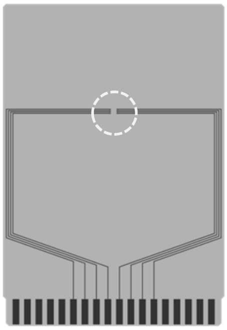
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. TMSOP8-A-Board-SD-1.0

SNT-8A Test Board

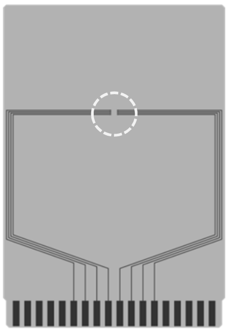
IC Mount Area

(1) Board A



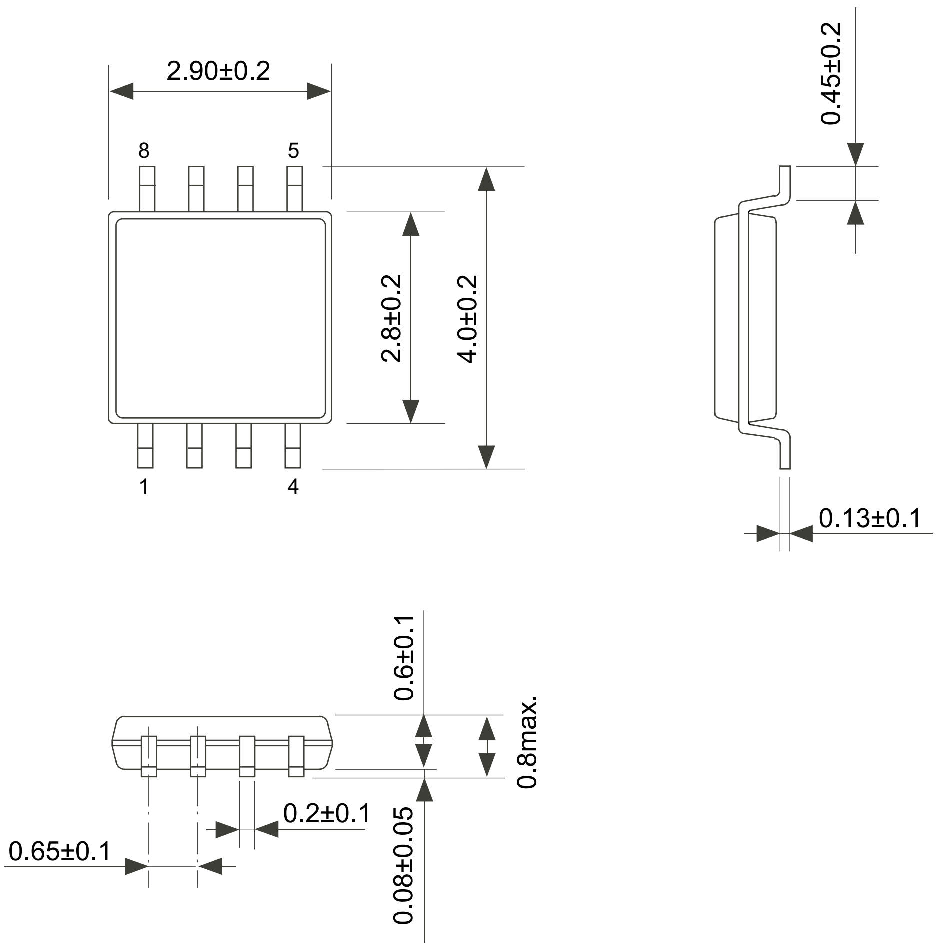
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

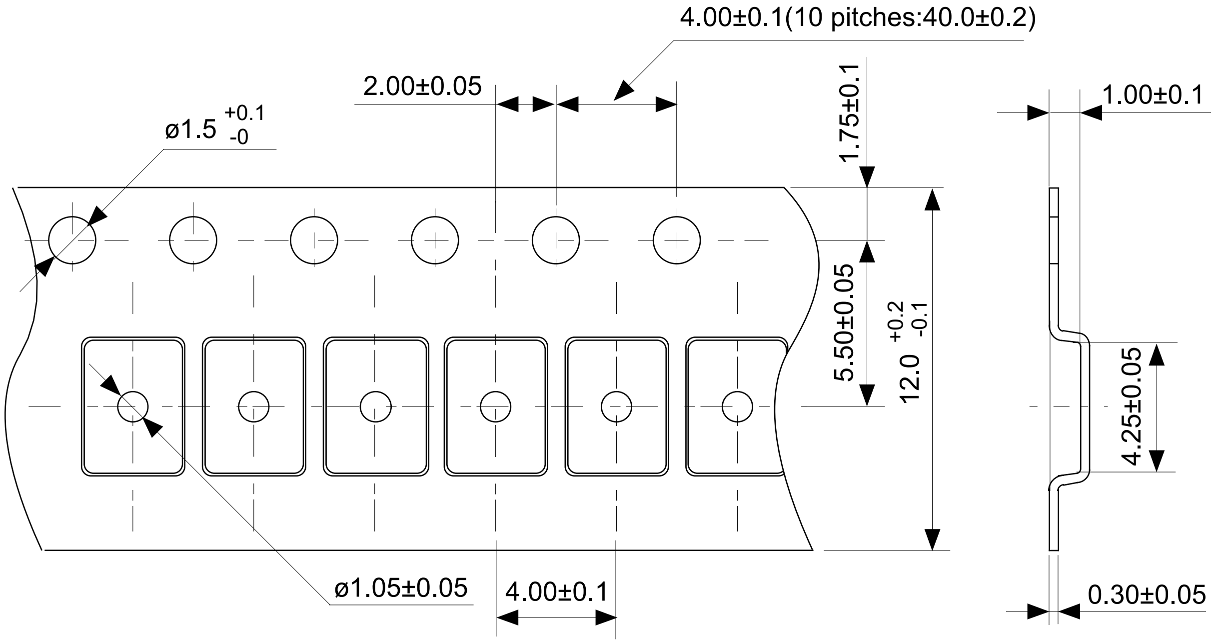
No. SNT8A-A-Board-SD-1.0

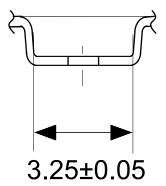


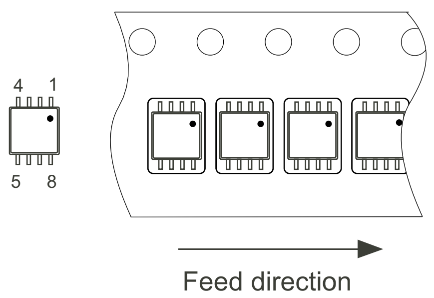
No. FM008-A-P-SD-1.2

TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.2
ANGLE	
UNIT	mm

ABLIC Inc.



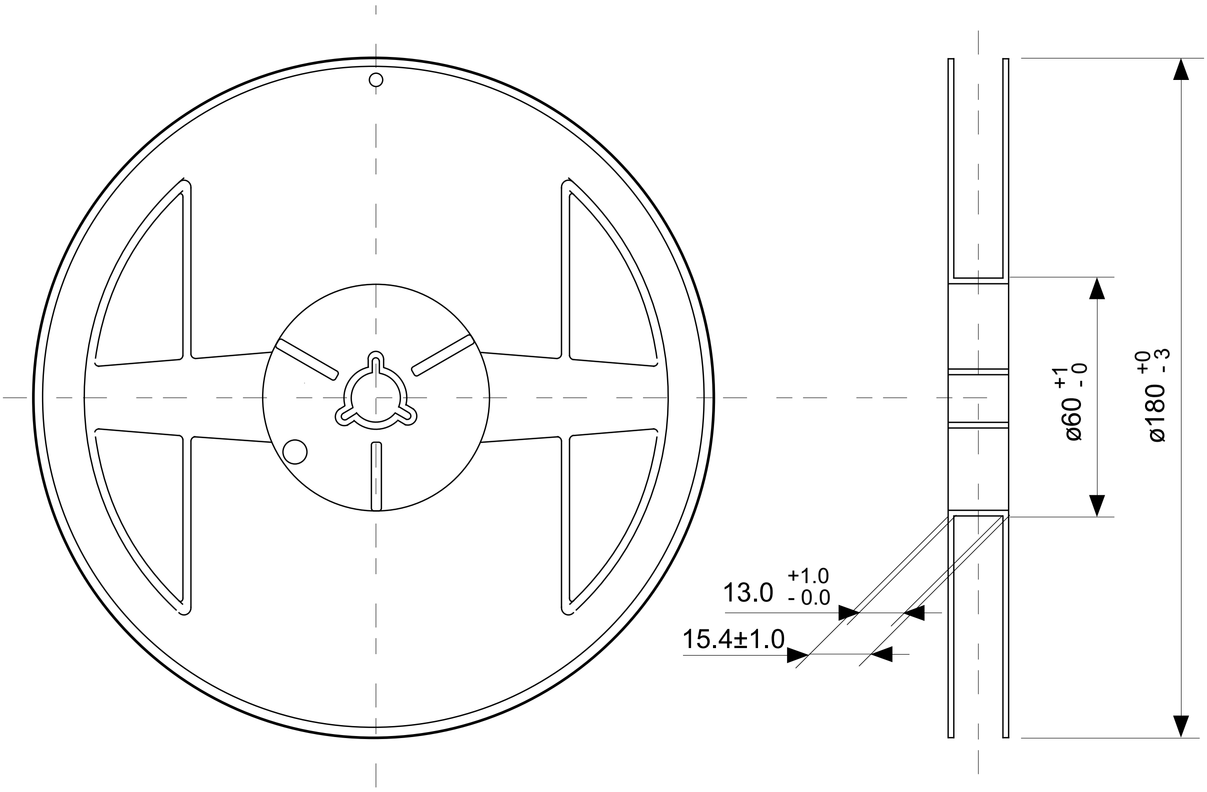




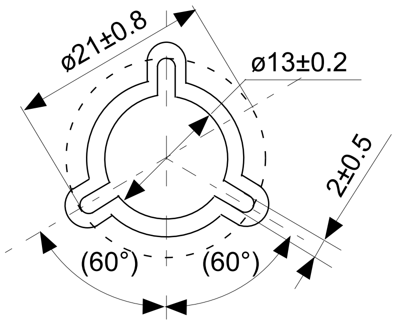
No. FM008-A-C-SD-3.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-3.0
ANGLE	
UNIT	mm

ABLIC Inc.

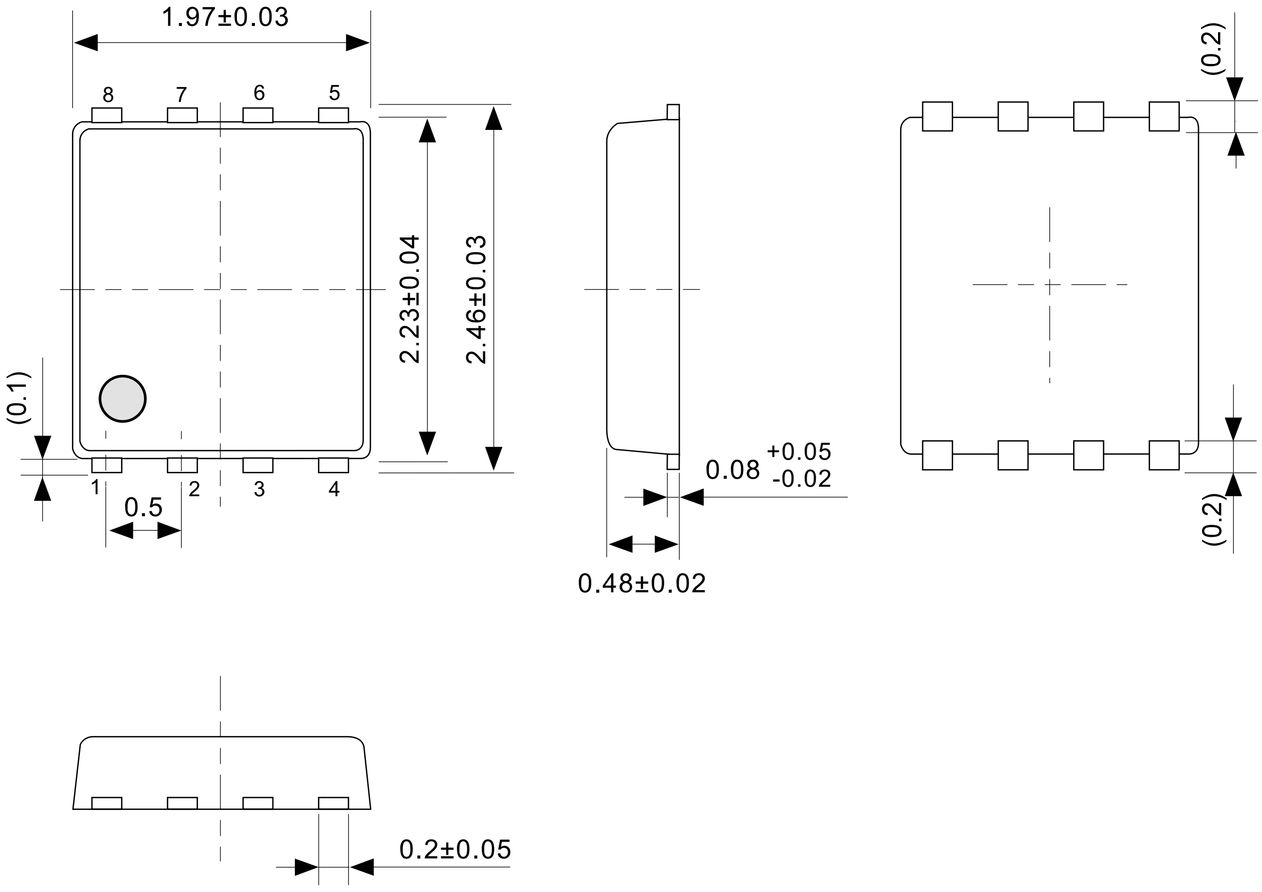


Enlarged drawing in the central part



No. FM008-A-R-SD-2.0

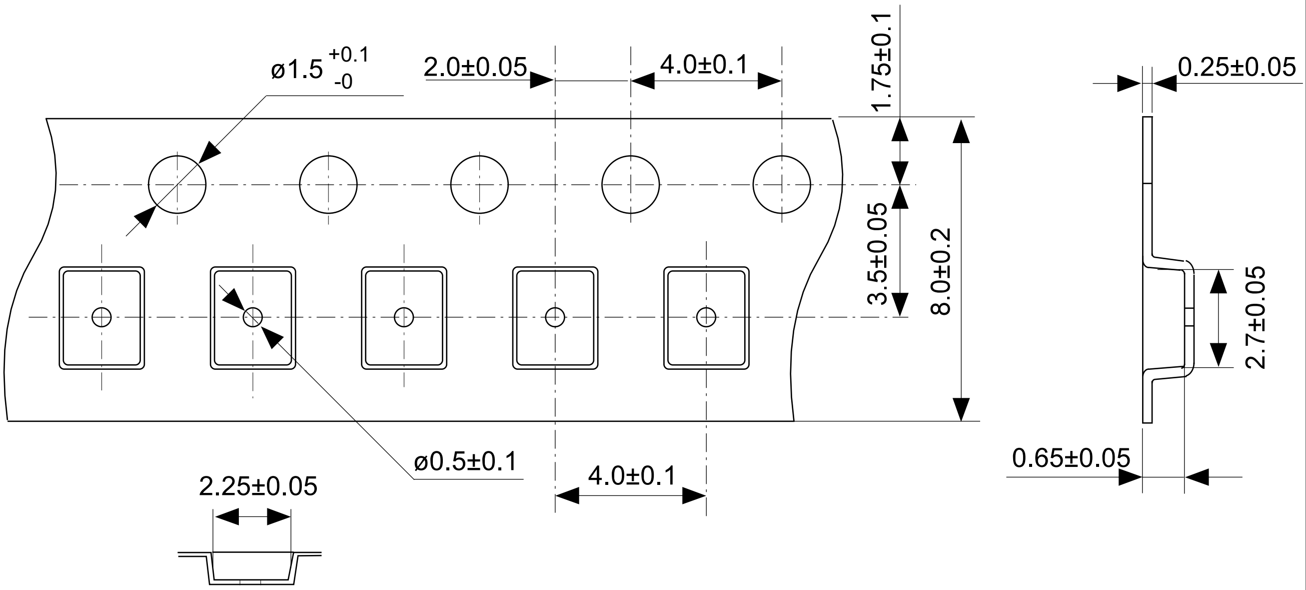
TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-2.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

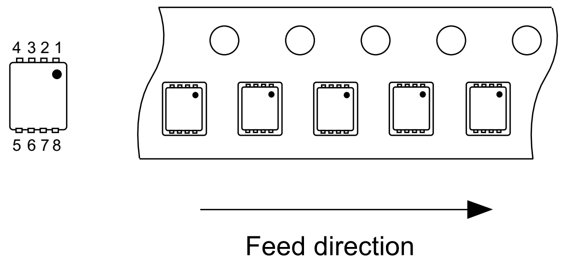


No. PH008-A-P-SD-2.1

TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.1
ANGLE	
UNIT	mm

ABLIC Inc.

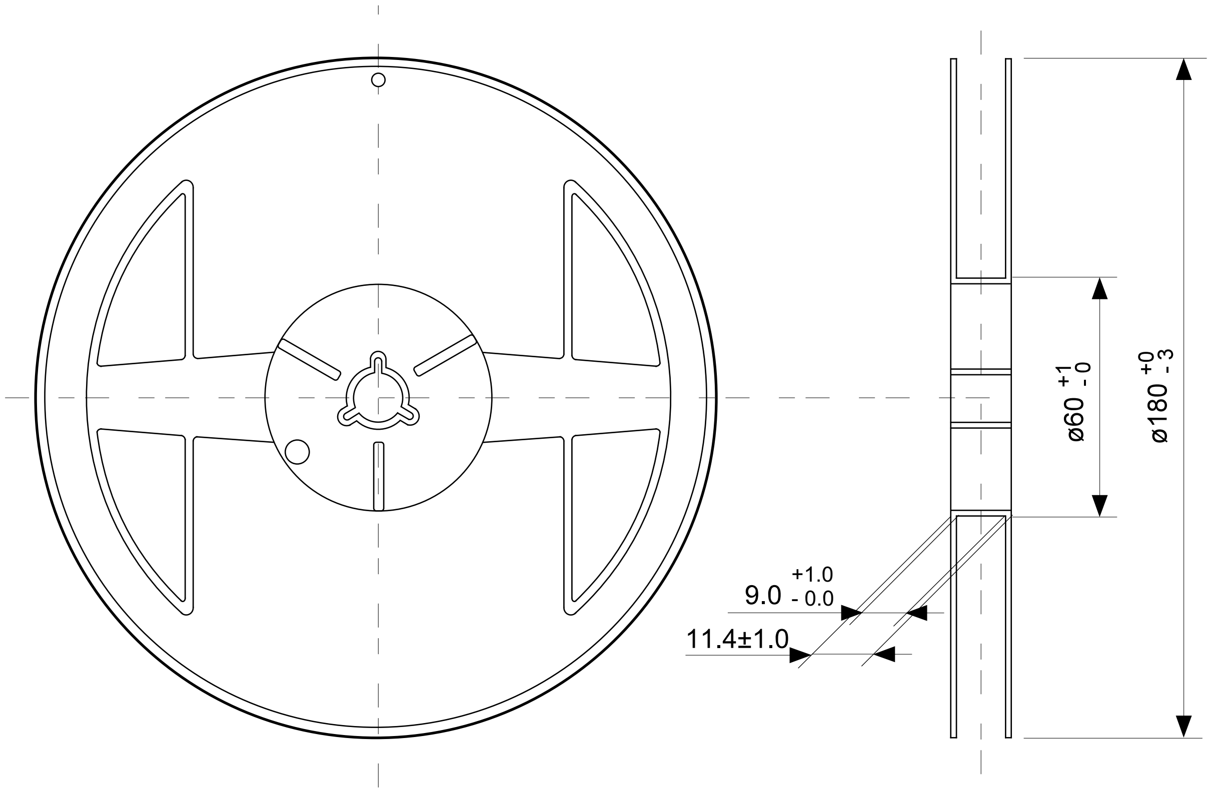




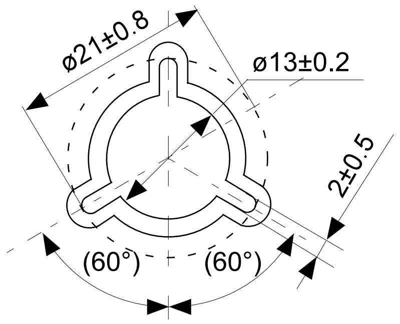
No. PH008-A-C-SD-2.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-2.0
ANGLE	
UNIT	mm

ABLIC Inc.



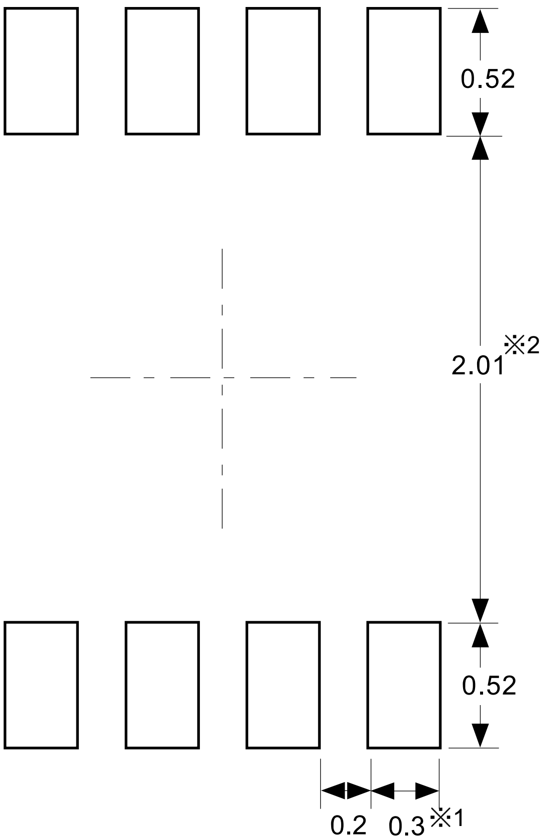
Enlarged drawing in the central part



No. PH008-A-R-SD-2.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-2.0		
ANGLE		QTY.	5,000
UNIT	mm		

ABLIC Inc.



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.96 mm ~ 2.06 mm)。

注意　1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝SNTパッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.96 mm to 2.06mm).

Caution　1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.96 mm ~ 2.06 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PH008-A-L-SD-4.1

TITLE	SNT-8A-A -Land Recommendation
No.	PH008-A-L-SD-4.1
ANGLE	
UNIT	mm

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2.4-2019.07