

The S-8255B Series is a monitoring IC for 3-serial to 5-serial cell lithium-ion rechargeable batteries, which includes high-accuracy voltage detection circuits and delay circuits. The S-8255B Series can monitor the status of 3-serial to 5-serial cell lithium-ion rechargeable battery packs.

Connecting an NTC, it allows for the temperature detection at four different points: high temperature detection during charging, low temperature detection during charging, high temperature detection during discharging, and low temperature detection during discharging.

## ■ Features

- High-accuracy voltage detection function for each cell
  - Overcharge detection voltage n (n = 1 to 5): 3.550 V to 4.600 V (50 mV step) Accuracy  $\pm 20$  mV
  - Overcharge release voltage n (n = 1 to 5): 3.150 V to 4.600 V<sup>\*1</sup> Accuracy  $\pm 50$  mV
  - Overdischarge detection voltage n (n = 1 to 5): 2.000 V to 3.200 V (100 mV step) Accuracy  $\pm 80$  mV
  - Overdischarge release voltage n (n = 1 to 5): 2.000 V to 3.400 V<sup>\*2</sup> Accuracy  $\pm 100$  mV
- Each delay time is settable by external capacitor (Temperature detection delay time is internally fixed)
- Independent control of charge inhibition, discharge inhibition, and power-saving by each control pin
- 0 V battery detection function is selectable: Available, unavailable
- CO and DO pin output voltage is limited to 8 V max. respectively
- Switching control for 3-serial to 5-serial cell is possible by inputting voltage to the SEL1 pin and the SEL2 pin
- Temperature detection is possible at four different points by connecting an NTC
  - High temperature detection ratio during charging / discharging: 0.600 to 0.900 (0.005 step) Accuracy  $\pm 0.005$
  - Low temperature detection ratio during charging / discharging: 0.030 to 0.400 (0.005 step) Accuracy  $\pm 0.005$
- High-withstand voltage: Absolute maximum rating 28 V
- Wide operation voltage range: 5 V to 24 V
- Wide operation temperature range: Ta =  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- Low current consumption
  - During operation: 19  $\mu\text{A}$  max. (Ta =  $+25^{\circ}\text{C}$ )
  - During power-saving: 0.1  $\mu\text{A}$  max. (Ta =  $+25^{\circ}\text{C}$ )
- Lead-free, halogen-free

\*1. Overcharge release voltage = Overcharge detection voltage – Overcharge hysteresis voltage  
(Overcharge hysteresis voltage n (n = 1 to 5) is selectable in 0 V to 0.4 V in 50 mV step)

\*2. Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage  
(Overdischarge hysteresis voltage n (n = 1 to 5) is selectable in 0 V to 0.7 V in 100 mV step)

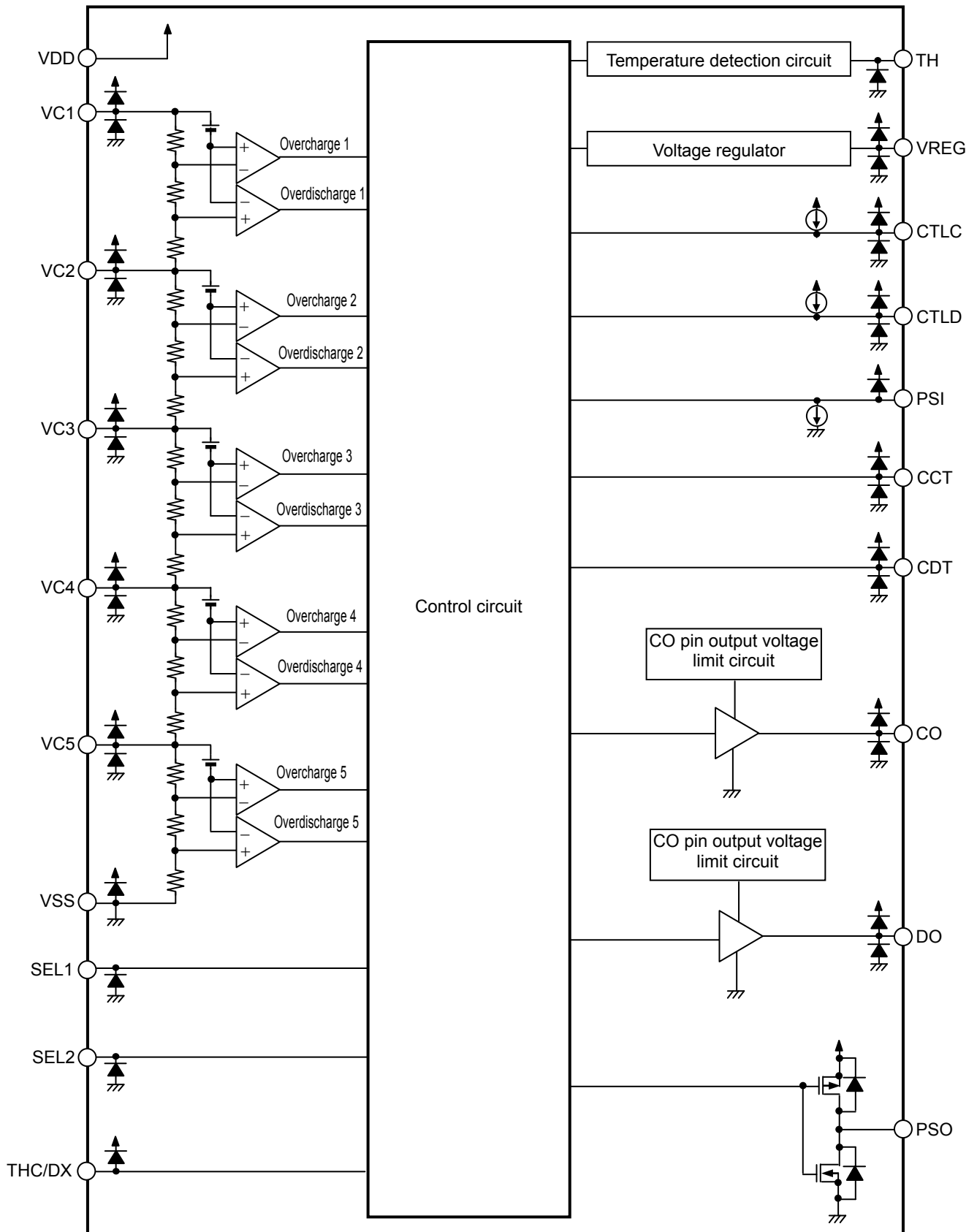
## ■ Application

- Rechargeable lithium-ion battery pack

## ■ Package

- 20-Pin TSSOP

■ **Block Diagram**

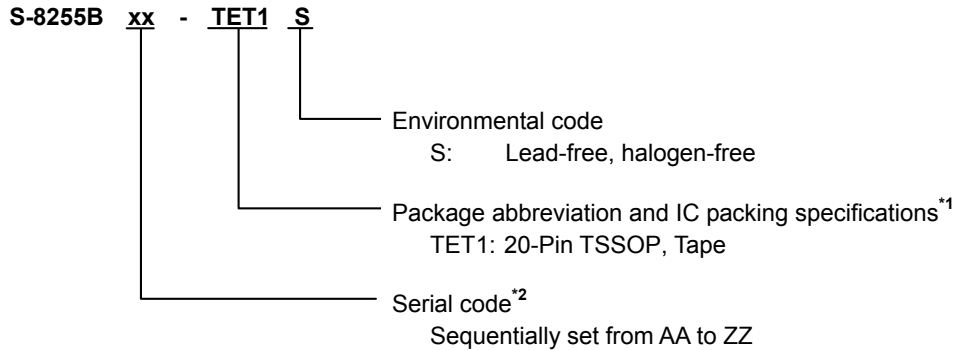


**Remark** Diodes in the figure are parasitic diodes.

**Figure 1**  
**ABLIC Inc.**

■ **Product Name Structure**

1. **Product name**



\*1. Refer to the tape drawing.  
 \*2. Refer to "3. Product name list".

2. **Package**

**Table 1 Package Drawing Code**

| Package Name | Dimension    | Tape         | Reel         |
|--------------|--------------|--------------|--------------|
| 20-Pin TSSOP | FT020-B-P-SD | FT020-B-C-SD | FT020-B-R-SD |

3. **Product name list**

**Table 2 (1 / 2)**

| Product Name    | Overcharge<br>Detection Voltage<br>[V <sub>CU</sub> ] | Overcharge<br>Release Voltage<br>[V <sub>CL</sub> ] | Overdischarge<br>Detection Voltage<br>[V <sub>DL</sub> ] | Overdischarge<br>Release Voltage<br>[V <sub>DU</sub> ] | 0 V Battery<br>Detection<br>Function*1 |
|-----------------|---|---|--|--|--|
| S-8255BAA-TET1S | 4.100 V   | 4.050 V   | 2.600 V  | 2.700 V  | Unavailable                            |
| S-8255BAB-TET1S | 4.250 V   | 4.150 V   | 2.500 V  | 3.000 V  | Available                              |

**Table 2 (2 / 2)**

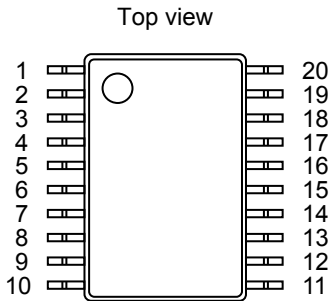
| Product Name    | High Temperature<br>Detection Ratio<br>during Charging<br>[r <sub>THCH</sub> ] | Low Temperature<br>Detection Ratio<br>during Charging<br>[r <sub>THCL</sub> ] | High Temperature<br>Detection Ratio<br>during Discharging<br>[r <sub>THDH</sub> ] | Low Temperature<br>Detection Ratio<br>during Discharging<br>[r <sub>THDL</sub> ] |
|-----------------|--|---|---|--|
| S-8255BAA-TET1S | 0.670  | 0.270   | 0.795   | 0.190  |
| S-8255BAB-TET1S | 0.670  | 0.270   | 0.795   | 0.190  |

\*1. 0 V battery detection function "available" / "unavailable" is selectable.

**Remark** Please contact our sales office for products other than those specified above.

■ **Pin Configuration**

1. **20-Pin TSSOP**



**Figure 2**

**Table 3**

| Pin No. | Symbol | Description  |
|---------|--------|--|
| 1       | TH     | Input pin for temperature detection  |
| 2       | VDD    | Input pin for positive power supply,<br>connection pin for positive voltage of battery 1   |
| 3       | VC1    | Connection pin for positive voltage of battery 1   |
| 4       | VC2    | Connection pin for negative voltage of battery 1,<br>connection pin for positive voltage of battery 2  |
| 5       | VC3    | Connection pin for negative voltage of battery 2,<br>connection pin for positive voltage of battery 3  |
| 6       | VC4    | Connection pin for negative voltage of battery 3,<br>connection pin for positive voltage of battery 4  |
| 7       | VC5    | Connection pin for negative voltage of battery 4,<br>connection pin for positive voltage of battery 5  |
| 8       | VSS    | Input pin for negative power supply,<br>connection pin for negative voltage of battery 5   |
| 9       | SEL1   | Switching pins for number of cells in series<br>[SEL1, SEL2] = ["L", "L"] : 5-serial cell<br>[SEL1, SEL2] = ["L", "H"] : 4-serial cell<br>[SEL1, SEL2] = ["H", "L"] : 3-serial cell<br>[SEL1, SEL2] = ["H", "H"] : Setting inhibited |
| 10      | SEL2   |  |
| 11      | CCT    | Capacitor connection pin for delay<br>for overcharge detection voltage   |
| 12      | CDT    | Capacitor connection pin for delay<br>for overdischarge detection voltage  |
| 13      | PSO    | Output pin for power-saving signal (CMOS output)   |
| 14      | DO     | Connection pin of discharge control FET gate (CMOS output)   |
| 15      | CO     | Connection pin of charge control FET gate (CMOS output)  |
| 16      | THC/DX | Switching pin for detection temperature  |
| 17      | CTLG   | Control pin for CO pin output  |
| 18      | CTLD   | Control pin for DO pin output  |
| 19      | PSI    | Control pin for Power-saving   |
| 20      | VREG   | Voltage output pin for temperature detection   |

■ Absolute Maximum Ratings

Table 4

(Ta = +25°C unless otherwise specified)

| Item                                      | Symbol           | Applied Pin  | Absolute Maximum Rating                        | Unit |
|---|------------------|--|--|------|
| Input voltage between VDD pin and VSS pin | V <sub>DS</sub>  | VDD  | V <sub>SS</sub> - 0.3 to V <sub>SS</sub> + 28  | V    |
| Input pin voltage                         | V <sub>IN</sub>  | VC1, VC2, VC3, VC4, VC5, CCT, CDT, SEL1, SEL2, TH, THC/DX, PSI, CTLC, CTLD | V <sub>SS</sub> - 0.3 to V <sub>DD</sub> + 0.3 | V    |
| Output pin voltage                        | V <sub>OUT</sub> | CO, DO, PSO, VREG  | V <sub>SS</sub> - 0.3 to V <sub>DD</sub> + 0.3 | V    |
| Operation ambient temperature             | T <sub>opr</sub> | -  | -40 to +85                                     | °C   |
| Storage temperature                       | T <sub>stg</sub> | -  | -40 to +125                                    | °C   |

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 5

| Item                                     | Symbol          | Condition    | Min.    | Typ. | Max. | Unit |      |
|--|-----------------|--------------|---------|------|------|------|------|
| Junction-to-ambient thermal resistance*1 | θ <sub>JA</sub> | 20-Pin TSSOP | Board A | -    | 68   | -    | °C/W |
|  |                 |              | Board B | -    | 59   | -    | °C/W |
|  |                 |              | Board C | -    | -    | -    | °C/W |
|  |                 |              | Board D | -    | -    | -    | °C/W |
|  |                 |              | Board E | -    | -    | -    | °C/W |

\*1. Test environment: compliance with JEDEC STANDARD JESD51-2A

**Remark** Refer to "■ Power Dissipation" and "Test Board" for details.

■ **Electrical Characteristics**

**Table 6 (1 / 2)**

(V1 = V2 = V3 = V4 = V5 = 3.5 V, Ta = +25°C unless otherwise specified)

| Item   | Symbol                        | Condition  | Min.                                | Typ.                        | Max.                                | Unit | Test Circuit |
|--|-------------------------------|--|-------------------------------------|-----------------------------|-------------------------------------|------|--------------|
| <b>Detection Voltage</b>                       |                               |  |                                     |                             |                                     |      |              |
| Overcharge detection voltage n (n = 1 to 5)    | V <sub>CU<sub>n</sub></sub>   | V1 = V2 = V3 = V4 = V5 = V <sub>CU<sub>n</sub></sub> - 0.050 V | V <sub>CU<sub>n</sub></sub> - 0.020 | V <sub>CU<sub>n</sub></sub> | V <sub>CU<sub>n</sub></sub> + 0.020 | V    | 1            |
| Overcharge release voltage n (n = 1 to 5)      | V <sub>CL<sub>n</sub></sub>   | -  | V <sub>CL<sub>n</sub></sub> - 0.050 | V <sub>CL<sub>n</sub></sub> | V <sub>CL<sub>n</sub></sub> + 0.050 | V    | 1            |
| Overdischarge detection voltage n (n = 1 to 5) | V <sub>DL<sub>n</sub></sub>   | -  | V <sub>DL<sub>n</sub></sub> - 0.080 | V <sub>DL<sub>n</sub></sub> | V <sub>DL<sub>n</sub></sub> + 0.080 | V    | 1            |
| Overdischarge release voltage n (n = 1 to 5)   | V <sub>DU<sub>n</sub></sub>   | -  | V <sub>DU<sub>n</sub></sub> - 0.100 | V <sub>DU<sub>n</sub></sub> | V <sub>DU<sub>n</sub></sub> + 0.100 | V    | 1            |
| <b>Delay Time Function*1</b>                   |                               |  |                                     |                             |                                     |      |              |
| CCT pin internal resistance                    | R <sub>CCT</sub>              | V1 = V <sub>CU</sub> + 0.025                                   | 6.15                                | 8.31                        | 10.20                               | MΩ   | 1            |
| CDT pin internal resistance                    | R <sub>CDT</sub>              | V1 = V <sub>DL</sub> - 0.085                                   | 615                                 | 831                         | 1020                                | kΩ   | 1            |
| CCT pin detection voltage                      | V <sub>CCT</sub>              | V1 = V <sub>CU</sub> + 0.025                                   | V <sub>DS</sub> × 0.68              | V <sub>DS</sub> × 0.70      | V <sub>DS</sub> × 0.72              | V    | 1            |
| CDT pin detection voltage                      | V <sub>CDT</sub>              | V1 = V <sub>DL</sub> - 0.085                                   | V <sub>DS</sub> × 0.68              | V <sub>DS</sub> × 0.70      | V <sub>DS</sub> × 0.72              | V    | 1            |
| <b>Input Voltage</b>                           |                               |  |                                     |                             |                                     |      |              |
| Operation voltage between VDD pin and VSS pin  | V <sub>DSOP</sub>             | Fixed output voltage of DO pin and CO pin                      | 5                                   | -                           | 24                                  | V    | -            |
| <b>Input Current</b>                           |                               |  |                                     |                             |                                     |      |              |
| Current consumption during operation           | I <sub>OPE</sub>              | -  | -                                   | 10                          | 19                                  | μA   | 1            |
| Current consumption during power-saving        | I <sub>PSV</sub>              | -  | -                                   | -                           | 0.1                                 | μA   | 1            |
| VC1 pin current                                | I <sub>VC1</sub>              | -  | -                                   | 0.25                        | 0.50                                | μA   | 1            |
| VC2 pin current                                | I <sub>VC2</sub>              | -  | -0.8                                | 0.0                         | 0.8                                 | μA   | 1            |
| VC3 pin current                                | I <sub>VC3</sub>              | -  | -0.8                                | 0.0                         | 0.8                                 | μA   | 1            |
| VC4 pin current                                | I <sub>VC4</sub>              | -  | -0.8                                | 0.0                         | 0.8                                 | μA   | 1            |
| VC5 pin current                                | I <sub>VC5</sub>              | -  | -0.8                                | 0.0                         | 0.8                                 | μA   | 1            |
| <b>Output Pin</b>                              |                               |  |                                     |                             |                                     |      |              |
| CO pin voltage "H"*2                           | V <sub>COH</sub>              | V <sub>COH</sub> < V <sub>DS</sub>                             | 4.0                                 | 6.0                         | 8.0                                 | V    | 1            |
| DO pin voltage "H"*3                           | V <sub>DOH</sub>              | V <sub>DOH</sub> < V <sub>DS</sub>                             | 4.0                                 | 6.0                         | 8.0                                 | V    | 1            |
| CO pin source current                          | I <sub>COH</sub>              | -  | 10                                  | -                           | -                                   | μA   | 1            |
| CO pin sink current                            | I <sub>COL</sub>              | V1 = V2 = V3 = V4 = V5 = 5.6 V                                 | 10                                  | -                           | -                                   | μA   | 1            |
| DO pin source current                          | I <sub>DOH</sub>              | -  | 10                                  | -                           | -                                   | μA   | 1            |
| DO pin sink current                            | I <sub>DOL</sub>              | -  | 10                                  | -                           | -                                   | μA   | 1            |
| PSO pin source current                         | I <sub>PSOH</sub>             | -  | 1                                   | -                           | 10                                  | μA   | 1            |
| PSO pin sink current                           | I <sub>PSOL</sub>             | V1 = V2 = V3 = V4 = V5 = 1.9 V                                 | 1                                   | -                           | 10                                  | μA   | 1            |
| <b>0 V Battery Detection Function</b>          |                               |  |                                     |                             |                                     |      |              |
| 0 V battery detection voltage n (n = 1 to 5)   | V <sub>0INH<sub>n</sub></sub> | 0 V battery detection function "available"                     | 1.0                                 | 1.3                         | 1.5                                 | V    | 1            |

\*1. Refer to "4. Delay time setting" in "■ Operation" for details of the delay time function.

\*2. When V<sub>COH</sub> ≥ V<sub>DS</sub>, V<sub>COH</sub> = V<sub>DD</sub>

\*3. When V<sub>DOH</sub> ≥ V<sub>DS</sub>, V<sub>DOH</sub> = V<sub>DD</sub>

**Remark** V<sub>DS</sub>: Input voltage between VDD pin and VSS pin (V1 + V2 + V3 + V4 + V5)

# BATTERY MONITORING IC FOR 3-SERIAL TO 5-SERIAL CELL PACK S-8255B Series

Rev.1.3\_00

**Table 6 (2 / 2)**

(V1 = V2 = V3 = V4 = V5 = 3.5 V, Ta = +25°C unless otherwise specified)

| Item  | Symbol             | Condition  | Min.                      | Typ.                  | Max.                      | Unit | Test Circuit |
|---|--------------------|--|---------------------------|-----------------------|---------------------------|------|--------------|
| <b>Control Pin</b>                                  |                    |  |                           |                       |                           |      |              |
| SEL1 pin voltage "H"                                | V <sub>SEL1H</sub> | –  | V <sub>DS</sub> × 0.95    | –                     | –                         | V    | –            |
| SEL2 pin voltage "H"                                | V <sub>SEL2H</sub> | –  | V <sub>DS</sub> × 0.95    | –                     | –                         | V    | –            |
| SEL1 pin voltage "L"                                | V <sub>SEL1L</sub> | –  | –                         | –                     | V <sub>DS</sub> × 0.05    | V    | –            |
| SEL2 pin voltage "L"                                | V <sub>SEL2L</sub> | –  | –                         | –                     | V <sub>DS</sub> × 0.05    | V    | –            |
| CTLC pin reverse voltage                            | V <sub>CTLC</sub>  | –  | 0.1                       | 0.7                   | 2.0                       | V    | 1            |
| CTLD pin reverse voltage                            | V <sub>CTLD</sub>  | –  | 0.1                       | 0.7                   | 2.0                       | V    | 1            |
| PSI pin reverse voltage                             | V <sub>PSI</sub>   | –  | 0.1                       | 4.0                   | 8.0                       | V    | 1            |
| CTLC pin response delay time                        | t <sub>CTLC</sub>  | –  | 0.275                     | 0.500                 | 0.725                     | ms   | 1            |
| CTLD pin response delay time                        | t <sub>CTLD</sub>  | –  | 0.275                     | 0.500                 | 0.725                     | ms   | 1            |
| PSI pin response delay time                         | t <sub>PSI</sub>   | –  | 0.3                       | 0.9                   | 3.0                       | ms   | 1            |
| CTLC pin current "H"                                | I <sub>CTLCH</sub> | –  | –0.1                      | 0.0                   | 0.1                       | μA   | 1            |
| CTLC pin current "L"                                | I <sub>CTLCL</sub> | –  | –0.45                     | –0.20                 | –0.05                     | μA   | 1            |
| CTLD pin current "H"                                | I <sub>CTLDH</sub> | –  | –0.1                      | 0.0                   | 0.1                       | μA   | 1            |
| CTLD pin current "L"                                | I <sub>CTLDL</sub> | –  | –0.45                     | –0.20                 | –0.05                     | μA   | 1            |
| PSI pin current "H"                                 | I <sub>PSIH</sub>  | –  | 0.0                       | 0.2                   | 0.4                       | μA   | 1            |
| PSI pin current "L"                                 | I <sub>PSIL</sub>  | –  | –0.1                      | 0.0                   | 0.1                       | μA   | 1            |
| <b>Temperature Detection Function</b>               |                    |  |                           |                       |                           |      |              |
| Output voltage for temperature detection            | V <sub>REG</sub>   | Voltage between VDD pin and VREG pin   | 4.0                       | 5.0                   | 6.0                       | V    | 2            |
| High temperature detection ratio during charging    | r <sub>THCH</sub>  | r <sub>THCH</sub> = (V <sub>REG</sub> – V <sub>TH</sub> ) / V <sub>REG</sub> | r <sub>THCH</sub> – 0.005 | r <sub>THCH</sub>     | r <sub>THCH</sub> + 0.005 | –    | 2            |
| Low temperature detection ratio during charging     | r <sub>THCL</sub>  | r <sub>THCL</sub> = (V <sub>REG</sub> – V <sub>TH</sub> ) / V <sub>REG</sub> | r <sub>THCL</sub> – 0.005 | r <sub>THCL</sub>     | r <sub>THCL</sub> + 0.005 | –    | 2            |
| High temperature detection ratio during discharging | r <sub>THDH</sub>  | r <sub>THDH</sub> = (V <sub>REG</sub> – V <sub>TH</sub> ) / V <sub>REG</sub> | r <sub>THDH</sub> – 0.005 | r <sub>THDH</sub>     | r <sub>THDH</sub> + 0.005 | –    | 2            |
| Low temperature detection ratio during discharging  | r <sub>THDL</sub>  | r <sub>THDL</sub> = (V <sub>REG</sub> – V <sub>TH</sub> ) / V <sub>REG</sub> | r <sub>THDL</sub> – 0.005 | r <sub>THDL</sub>     | r <sub>THDL</sub> + 0.005 | –    | 2            |
| THC/DX pin voltage "H"                              | V <sub>THH</sub>   | –  | V <sub>DS</sub> – 2.0     | V <sub>DS</sub> – 1.5 | V <sub>DS</sub> – 1.0     | V    | 2            |
| THC/DX pin voltage "L"                              | V <sub>THL</sub>   | –  | 0.5                       | 1.0                   | 1.5                       | V    | 2            |
| Temperature detection delay time                    | t <sub>TH</sub>    | –  | 1.0                       | 2.0                   | 3.0                       | s    | 2            |

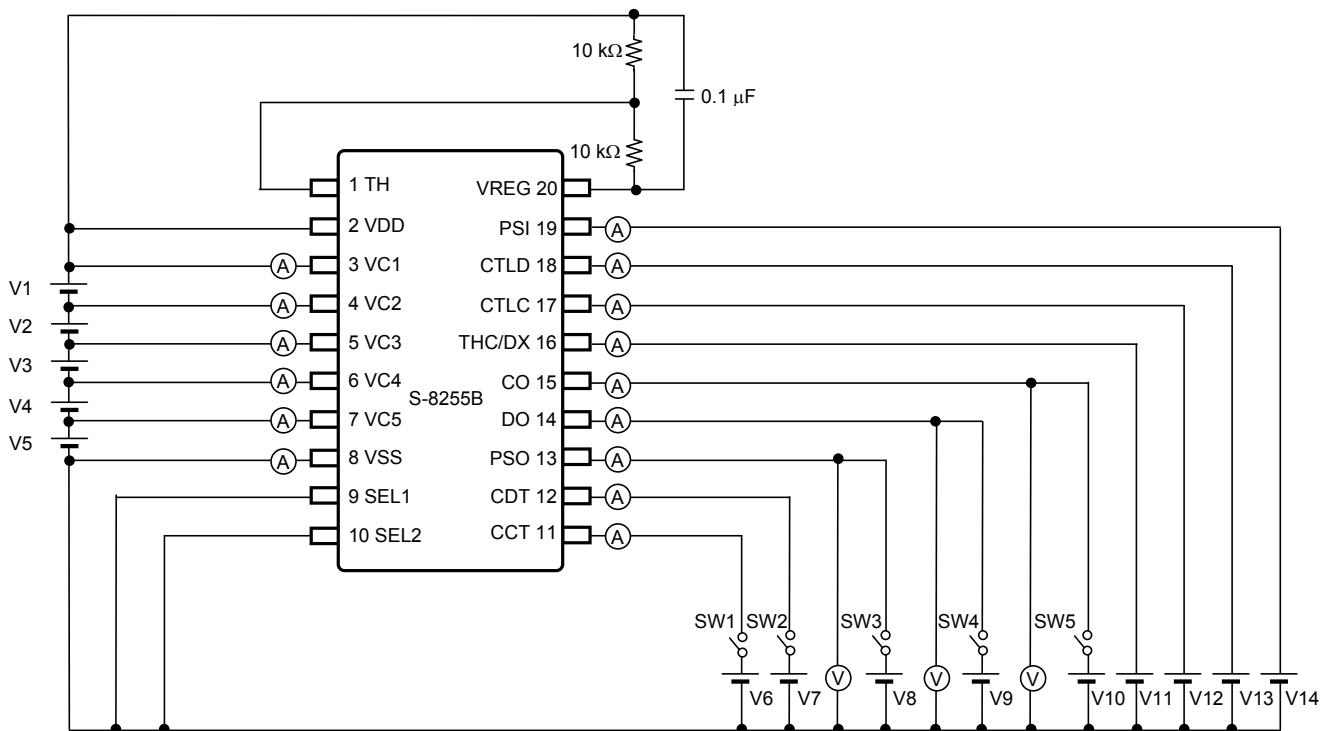
■ **Test Circuits**

Unless otherwise specified, for the CO pin output voltage ( $V_{CO}$ ), DO pin output voltage ( $V_{DO}$ ), and PSO pin output voltage ( $V_{PSO}$ ), "L" or "H" is judged as follows.

- L :  $[V_{CO}, V_{DO}, V_{PSO}] \leq V_{DS} \times 0.1 V$
- H :  $[V_{CO}, V_{DO}, V_{PSO}] > V_{DS} \times 0.1 V$

**Remark**  $V_{DS}$ : Input voltage between VDD pin and VSS pin ( $V1 + V2 + V3 + V4 + V5$ )

**1. Test circuit 1**



**Figure 3 Test Circuit 1**

This section provides explanations of Test items using Test circuit 1. Perform each test after setting as shown in Table 7.

**Table 7 Initial Setting of Test Circuit 1 (1 / 2)**

| V1    | V2    | V3    | V4    | V5    | V6 | V7 | V8 | V9 | V10 |
|-------|-------|-------|-------|-------|----|----|----|----|-----|
| 3.5 V | 3.5 V | 3.5 V | 3.5 V | 3.5 V | -  | -  | -  | -  | -   |

**Table 7 Initial Setting of Test Circuit 1 (2 / 2)**

| V11 | V12      | V13      | V14      | SW1 | SW2 | SW3 | SW4 | SW5 |
|-----|----------|----------|----------|-----|-----|-----|-----|-----|
| 0 V | $V_{DS}$ | $V_{DS}$ | $V_{DS}$ | OFF | OFF | OFF | OFF | OFF |



**1.1 Overcharge detection voltage n ( $V_{CU_n}$ ), overcharge release voltage n ( $V_{CL_n}$ )**

When the voltage V1 is gradually increased after setting  $V1 = V2 = V3 = V4 = V5 = V_{CU_n} - 0.05 \text{ V}$  and  $V_{CO}$  changes from "H" to "L", V1 is defined as the overcharge detection voltage 1 ( $V_{CU1}$ ). When the voltage V1 is then gradually decreased and  $V_{CO}$  changes from "L" to "H", V1 is defined as the overcharge release voltage 1 ( $V_{CL1}$ ). Overcharge detection voltage n ( $V_{CU_n}$ ) and overcharge release voltage n ( $V_{CL_n}$ ) (n = 2 to 5) can be determined in the same way as when n = 1.

**1.2 Overdischarge detection voltage n ( $V_{DL_n}$ ), overdischarge release voltage n ( $V_{DU_n}$ )**

When the voltage V1 is gradually decreased and  $V_{DO}$  changes from "H" to "L", V1 is defined as the overdischarge detection voltage 1 ( $V_{DL1}$ ). When the voltage V1 is then gradually increased and  $V_{DO}$  changes from "L" to "H", V1 is defined as the overdischarge release voltage 1 ( $V_{DU1}$ ). Overdischarge detection voltage n ( $V_{DL_n}$ ) and overdischarge release voltage n ( $V_{DU_n}$ ) (n = 2 to 5) can be determined in the same way as when n = 1.

**1.3 CCT pin internal resistance ( $R_{CCT}$ ), CCT pin detection voltage ( $V_{CCT}$ )**

The CCT pin internal resistance ( $R_{CCT}$ ) is defined by  $R_{CCT} = V_{DS} / I_{CCT}$  under the set conditions of  $V1 = V_{CU1} + 0.025 \text{ V}$  after setting  $V6 = 0 \text{ V}$  and setting SW1 to ON. When the voltage V6 is then gradually increased and  $V_{CO}$  changes from "H" to "L", V6 is defined as the CCT pin detection voltage ( $V_{CCT}$ ).

**1.4 CDT pin internal resistance ( $R_{CDT}$ ), CDT pin detection voltage ( $V_{CDT}$ )**

The CDT pin internal resistance ( $R_{CDT}$ ) is defined by  $R_{CDT} = V_{DS} / I_{CDT}$  under the set conditions of  $V1 = V_{DL1} - 0.085 \text{ V}$  after setting  $V7 = 0 \text{ V}$  and setting SW2 to ON. When the voltage V7 is then gradually increased and  $V_{DO}$  changes from "H" to "L", V7 is defined as the CDT pin detection voltage ( $V_{CDT}$ ).

**1.5 Current consumption during operation ( $I_{OPE}$ )**

The current consumption during operation ( $I_{OPE}$ ) is  $I_{VSS}$  under the initial setting shown in **Table 7**.

**1.6 Current consumption during power-saving ( $I_{PSV}$ )**

The current consumption during power-saving ( $I_{PSV}$ ) is  $I_{VSS}$  when  $V14 = 0 \text{ V}$ .

**1.7 CO pin source current ( $I_{COH}$ )**

The CO pin source current ( $I_{COH}$ ) is  $I_{CO}$  when  $V10 = V_{COH} - 0.5 \text{ V}$  and SW5 is ON.

**1.8 CO pin sink current ( $I_{COL}$ )**

The CO pin sink current ( $I_{COL}$ ) is  $I_{CO}$  when  $V1 = V2 = V3 = V4 = V5 = 4.6 \text{ V}$ ,  $V10 = 0.5 \text{ V}$ , and SW5 is ON.

**1.9 DO pin source current ( $I_{DOH}$ )**

The DO pin source current ( $I_{DOH}$ ) is  $I_{DO}$  when  $V9 = V_{DOH} - 0.5 \text{ V}$  and SW4 is ON.

**1.10 DO pin sink current ( $I_{DOL}$ )**

The DO pin sink current ( $I_{DOL}$ ) is  $I_{DO}$  when  $V1 = V2 = V3 = V4 = V5 = 1.9 \text{ V}$ ,  $V9 = 0.5 \text{ V}$ , and SW4 is ON.

**1.11 PSO pin source current ( $I_{PSOH}$ )**

The PSO pin source current ( $I_{PSOH}$ ) is  $I_{PSO}$  when  $V14 = 0 \text{ V}$ ,  $V8 = V_{DS} - 0.5 \text{ V}$ , and SW3 is ON.

**1.12 PSO pin sink current ( $I_{PSOL}$ )**

The PSO pin sink current ( $I_{PSOL}$ ) is  $I_{PSO}$  when  $V8 = 0.5 \text{ V}$  and SW3 is ON.

**1.13 0 V battery detection voltage n ( $V_{0INHn}$ ) (0 V battery detection function "available")**

When the voltage V1 is gradually decreased and  $V_{CO}$  changes from "H" to "L", V1 is defined as the 0 V battery detection voltage 1 ( $V_{0INH1}$ ).

0 V battery detection voltage n ( $V_{0INHn}$ ) (n = 2 to 5) can be determined in the same way as when n = 1.

**1.14 CTLC pin reverse voltage ( $V_{CTLC}$ )**

When the voltage V12 is gradually decreased and  $V_{CO}$  changes from "H" to "L", V12 is defined as the CTLC pin reverse voltage ( $V_{CTLC}$ ).

**1.15 CTLD pin reverse voltage ( $V_{CTLD}$ )**

When the voltage V13 is gradually decreased and  $V_{DO}$  changes from "H" to "L", V13 is defined as the CTLD pin reverse voltage ( $V_{CTLD}$ ).

**1.16 PSI pin reverse voltage ( $V_{PSI}$ )**

When the voltage V14 is gradually decreased and  $V_{PSO}$  changes from "L" to "H", V14 is defined as the PSI pin reverse voltage ( $V_{PSI}$ ).

**1.17 CTLC pin response delay time ( $t_{CTLC}$ )**

The CTLC pin response delay time ( $t_{CTLC}$ ) is the time period from when the voltage V12 changes to V12 = 0 V until when  $V_{CO}$  changes from "H" to "L".

**1.18 CTLD pin response delay time ( $t_{CTLD}$ )**

The CTLD pin response delay time ( $t_{CTLD}$ ) is the time period from when the voltage V13 changes to V13 = 0 V until when  $V_{DO}$  changes from "H" to "L".

**1.19 PSI pin response delay time ( $t_{PSI}$ )**

The PSI pin response delay time ( $t_{PSI}$ ) is the time period from when the voltage V14 changes to V14 = 0 V until when  $V_{PSO}$  changes from "L" to "H".

**1.20 CTLC pin current "H" ( $I_{CTLCH}$ ), CTLC pin current "L" ( $I_{CTLCL}$ )**

The CTLC pin current "H" ( $I_{CTLCH}$ ) is  $I_{CTLC}$  when V12 =  $V_{DS}$ .

The CTLC pin current "L" ( $I_{CTLCL}$ ) is  $I_{CTLC}$  when V12 = 0 V.

**1.21 CTLD pin current "H" ( $I_{CTLDH}$ ), CTLD pin current "L" ( $I_{CTLDL}$ )**

The CTLD pin current "H" ( $I_{CTLDH}$ ) is  $I_{CTLD}$  when V13 =  $V_{DS}$ .

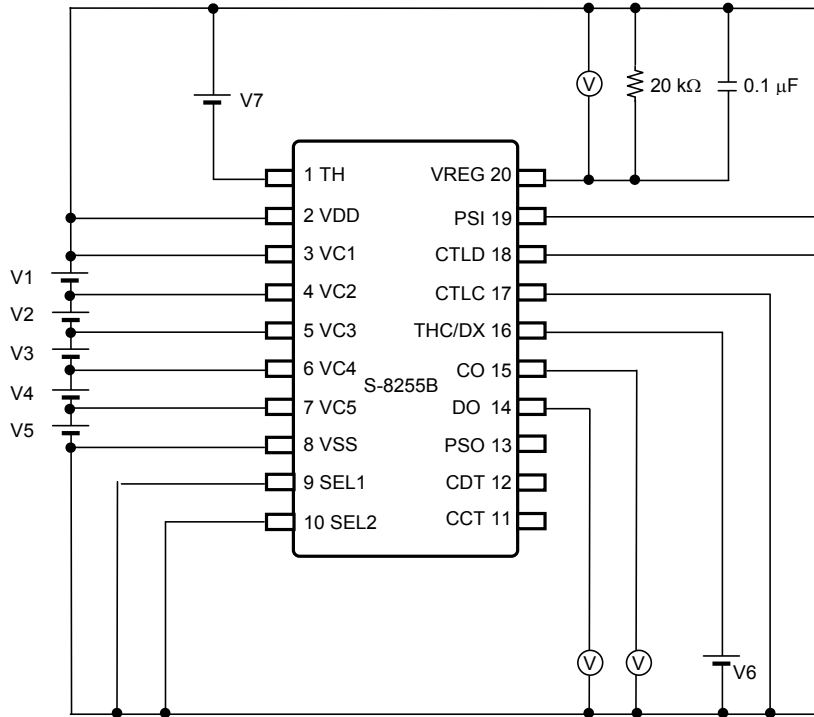
The CTLD pin current "L" ( $I_{CTLDL}$ ) is  $I_{CTLD}$  when V13 = 0 V.

**1.22 PSI pin current "H" ( $I_{PSIH}$ ), PSI pin current "L" ( $I_{PSIL}$ )**

The PSI pin current "H" ( $I_{PSIH}$ ) is  $I_{PSI}$  when V14 =  $V_{DS}$ .

The PSI pin current "L" ( $I_{PSIL}$ ) is  $I_{PSI}$  when V14 = 0 V.

**2. Test circuit 2**



**Figure 4 Test Circuit 2**

This section provides explanations of Test items using Test circuit 2.  
 Perform each test after setting as shown in **Table 8**.

**Table 8 Initial Setting of Test Circuit 2**

| V1    | V2    | V3    | V4    | V5    | V6  | V7 <sup>*1</sup> |
|-------|-------|-------|-------|-------|-----|------------------|
| 3.5 V | 3.5 V | 3.5 V | 3.5 V | 3.5 V | 0 V | 2.5 V            |

\*1. V7 is an absolute value.

**2.1 Output voltage for temperature detection ( $V_{REG}$ )**

The maximum voltage between the VDD pin and VREG pin is defined as the output voltage for temperature detection ( $V_{REG}$ ).

**2.2 High temperature detection ratio during charging ( $r_{THCH}$ )**

When the voltage V7 is gradually decreased after setting  $V6 = V_{DS}$  and  $V_{CO}$  changes from "H" to "L", the high temperature detection ratio during charging ( $r_{THCH}$ ) is defined by  $(V_{REG} - V7) / V_{REG}$ .

**2.3 Low temperature detection ratio during charging ( $r_{THCL}$ )**

When the voltage V7 is gradually increased after setting  $V6 = V_{DS}$  and  $V_{CO}$  changes from "H" to "L", the low temperature detection ratio during charging ( $r_{THCL}$ ) is defined by  $(V_{REG} - V7) / V_{REG}$ .

**2.4 High temperature detection ratio during discharging ( $r_{THDH}$ )**

When the voltage V7 is gradually decreased and  $V_{CO}$  changes from "H" to "L" and  $V_{DO}$  changes from "H" to "L", the high temperature detection ratio during discharging ( $r_{THDH}$ ) is defined by  $(V_{REG} - V7) / V_{REG}$ .

**2.5 Low temperature detection ratio during discharging ( $r_{THDL}$ )**

When the voltage V7 is gradually increased and  $V_{CO}$  changes from "H" to "L" and  $V_{DO}$  changes from "H" to "L", the low temperature detection ratio during discharging ( $r_{THDL}$ ) is defined by  $(V_{REG} - V7) / V_{REG}$ .

**2.6 THC/DX pin voltage "H" ( $V_{THH}$ )**

When the voltage V6 is gradually increased after setting  $(1 - r_{THDH}) \times V_{REG} < V7 < (1 - r_{THCH}) \times V_{REG}$  and  $V_{DO}$  changes from "L" to "H", V6 is defined as the THC/DX pin voltage "H" ( $V_{THH}$ ).

**2.7 THC/DX pin voltage "L" ( $V_{THL}$ )**

When the voltage V6 is gradually decreased after setting  $(1 - r_{THDH}) \times V_{REG} < V7 < (1 - r_{THCH}) \times V_{REG}$  and  $V_{DO}$  changes from "H" to "L", V6 is defined as the THC/DX pin voltage "L" ( $V_{THL}$ ).

**2.8 Temperature detection delay time ( $t_{TH}$ )**

The temperature detection delay time ( $t_{TH}$ ) is the time period from when the voltage V7 changes to 0 V until when  $V_{CO}$  changes from "H" to "L" and  $V_{DO}$  changes from "H" to "L".

## ■ Operation

**Remark** Refer to "■ Connection Examples of Battery Protection IC".

### 1. Normal status

The status when CO pin output voltage ( $V_{CO}$ ) = "H", DO pin output voltage ( $V_{DO}$ ) = "H" and PSO pin output voltage ( $V_{PSO}$ ) = "L" is the normal status.

All the conditions mentioned below should be satisfied for returning to the normal status.

- The voltage of each of the batteries is in the range from overcharge detection voltage n ( $V_{CUn}$ ) to overdischarge detection voltage n ( $V_{DLn}$ ).
- CTLC pin voltage, CTLD pin voltage, and PSI pin voltage are higher than CTLC pin reverse voltage ( $V_{CTLC}$ ), CTLD pin reverse voltage ( $V_{CTLD}$ ), and PSI pin reverse voltage ( $V_{PSI}$ ), respectively.
- Either (1) or (2) below is satisfied for TH pin voltage ( $V_{TH}$ ).

$$(1) \text{ When } V_{THC/DX} \geq V_{THH}: (1 - \Gamma_{THCH}) \times V_{REG} < V_{TH} < (1 - \Gamma_{THCL}) \times V_{REG}$$

$$(2) \text{ When } V_{THC/DX} \leq V_{THL}: (1 - \Gamma_{THDH}) \times V_{REG} < V_{TH} < (1 - \Gamma_{THDL}) \times V_{REG}$$

**Caution** After the battery is connected, there may be cases when discharging cannot be performed. In this case, the S-8255B Series returns to the normal status when the following condition is satisfied.

- Changing the PSI pin voltage to be  $V_{DS} \rightarrow 0V \rightarrow V_{DS}$

**Remark**

- $V_{THC/DX}$ : THC/DX pin voltage
- $V_{THH}$ : THC/DX pin voltage "H"
- $V_{THL}$ : THC/DX pin voltage "L"
- $\Gamma_{THCH}$ : High temperature detection ratio during charging
- $\Gamma_{THCL}$ : Low temperature detection ratio during charging
- $\Gamma_{THDH}$ : High temperature detection ratio during discharging
- $\Gamma_{THDL}$ : Low temperature detection ratio during discharging
- $V_{REG}$ : Output voltage for temperature detection
- $V_{DS}$ : Input voltage between VDD pin and VSS pin ( $V1 + V2 + V3 + V4 + V5$ )

### 2. Overcharge status

When the voltage of any of the batteries exceeds the overcharge detection voltage n ( $V_{CUn}$ ) and the status continues for the overcharge detection delay time ( $t_{CU}$ )\*1 or longer, the CO pin changes to the  $V_{SS}$  level. This is the overcharge status.

The overcharge status is released if the following condition is satisfied.

- Voltage of battery  $\leq V_{CLn}$

\*1. Refer to "4. Delay time setting" for details.

**Remark**  $V_{CLn}$ : Overcharge release voltage n (n = 1 to 5)

### 3. Overdischarge status

When the voltage of any of the batteries falls below the overdischarge detection voltage  $n$  ( $V_{DLn}$ ) and the status continues for the overdischarge detection delay time ( $t_{DL}$ )<sup>\*1</sup> or longer, the DO pin changes to the  $V_{SS}$  level. This is the overdischarge status.

The overdischarge status is released if the following condition is satisfied.

- Voltage of battery  $\geq V_{DUn}$

\*1. Refer to "4. Delay time setting" for details.

**Remark**  $V_{DUn}$ : Overdischarge release voltage  $n$  ( $n = 1$  to  $5$ )

### 4. Delay time setting

Users are able to set delay time for the period from when the S-8255B Series detects change in the voltage of any of the batteries until when it outputs to the CO pin or DO pin. Each delay time is determined by a resistor in the S-8255B Series and an external capacitor.

In the overcharge detection, when the voltage of any of the batteries exceeds overcharge detection voltage  $n$  ( $V_{CU_n}$ ), the S-8255B Series starts charging to the CCT pin's capacitor ( $C_{CCT}$ ) via the CCT pin internal resistance ( $R_{CCT}$ ). After a certain period, the CO pin changes to the  $V_{SS}$  level when the voltage at the CCT pin reaches the CCT pin detection voltage ( $V_{CCT}$ ). This period is overcharge detection delay time ( $t_{CU}$ ).

$t_{CU}$  is calculated using the following equation.

$$\begin{aligned} t_{CU} [s] &= -\ln(1 - V_{CCT} / V_{DS}) \times C_{CCT} [\mu F] \times R_{CCT} [M\Omega] \\ &= -\ln(1 - 0.7 \text{ typ.}) \times C_{CCT} [\mu F] \times 8.31 [M\Omega] \text{ typ.} \\ &= 10.0 [M\Omega] \text{ typ.} \times C_{CCT} [\mu F] \end{aligned}$$

Overdischarge detection delay time ( $t_{DL}$ ) is calculated using the following equations as well.

$$t_{DL} [ms] = -\ln(1 - V_{CDT} / V_{DS}) \times C_{CDT} [\mu F] \times R_{CDT} [k\Omega]$$

When  $C_{CCT} = C_{CDT} = 0.1 [\mu F]$ , each delay time is calculated as follows.

$$\begin{aligned} t_{CU} [s] &= 10.0 [M\Omega] \text{ typ.} \times 0.1 [\mu F] = 1.0 [s] \text{ typ.} \\ t_{DL} [ms] &= 1000 [k\Omega] \text{ typ.} \times 0.1 [\mu F] = 100 [ms] \text{ typ.} \end{aligned}$$

**Remark**  $V_{DS}$ : Input voltage between VDD pin and VSS pin ( $V1 + V2 + V3 + V4 + V5$ )

### 5. 0 V Battery detection function

For detection function of self-discharged battery (0 V battery), "available" / "unavailable" is selectable.

- 0 V battery detection function "available"  
The voltage  $V_{CO}$  changes to the  $V_{SS}$  level when the voltage of any of the batteries is  $V_{0INHn}$  or lower.

**Caution** When the VDD pin voltage is lower than the minimum value of operation voltage between VDD pin and VSS pin ( $V_{DSOP}$ ), the S-8255B Series' operation is not assured.

**Remark**  $V_{0INHn}$ : 0 V battery detection voltage  $n$  ( $n = 1$  to  $5$ )  
 $V_{CO}$ : CO pin voltage

## 6. SEL1 pin and SEL2 pin

Switching control for 3-serial to 5-serial cell is possible by inputting voltage to the SEL1 pin and to the SEL2 pin. Be sure to use the SEL1 pin and the SEL2 pin at the "H" or "L" level.

**Table 9 Settings of SEL1 Pin and SEL2 Pin**

| SEL1 Pin | SEL2 Pin | Setting                  |
|----------|----------|--------------------------|
| "L"      | "L"      | 5-serial cell monitoring |
| "L"      | "H"      | 4-serial cell monitoring |
| "H"      | "L"      | 3-serial cell monitoring |
| "H"      | "H"      | Setting inhibited        |

**Remark** "H" is the status when  $V_{SEL1} \geq V_{SEL1H}$ ,  $V_{SEL2} \geq V_{SEL2H}$ , and "L" is the status when  $V_{SEL1} \leq V_{SEL1L}$ ,  $V_{SEL2} \leq V_{SEL2L}$ .

$V_{SEL1H}$ : SEL1 pin voltage "H"

$V_{SEL2H}$ : SEL2 pin voltage "H"

$V_{SEL1L}$ : SEL1 pin voltage "L"

$V_{SEL2L}$ : SEL2 pin voltage "L"

## 7. CTLC pin and CTLD pin

The CTLC pin controls the CO pin, and the CTLD pin controls the DO pin. Thus it is possible for users to control the CO pin and the DO pin respectively. These controls precede the battery monitoring circuit.

**Table 10 Status Set by CTLC Pin**

| CTLC Pin  | CO Pin         |
|---|----------------|
| $V_{SS} \text{ level} \leq \text{CTLC pin voltage} < V_{CTLC}$    | $V_{SS}$ level |
| $V_{CTLC} \leq \text{CTLC pin voltage} \leq V_{DD} \text{ level}$ | "H"            |

**Remark**  $V_{CTLC}$ : CTLC pin reverse voltage

**Table 11 Status Set by CTLD Pin**

| CTLD Pin  | DO Pin         |
|---|----------------|
| $V_{SS} \text{ level} \leq \text{CTLD pin voltage} < V_{CTLD}$    | $V_{SS}$ level |
| $V_{CTLD} \leq \text{CTLD pin voltage} \leq V_{DD} \text{ level}$ | "H"            |

**Remark**  $V_{CTLD}$ : CTLD pin reverse voltage

## 8. PSI pin

When the PSI pin is activated, the power-saving function starts to operate, and most operations halt. In this case, the CO pin and DO pin change to the  $V_{SS}$  level, and the PSO pin changes to the  $V_{DD}$  level.

**Table 12 Status Set by PSI Pin**

| PSI Pin   | CO Pin         | DO Pin         | PSO Pin        |
|---|----------------|----------------|----------------|
| $V_{PSI} < \text{PSI pin voltage} \leq V_{DD} \text{ level}$    | "H"            | "H"            | $V_{SS}$ level |
| $V_{SS} \text{ level} \leq \text{PSI pin voltage} \leq V_{PSI}$ | $V_{SS}$ level | $V_{SS}$ level | $V_{DD}$ level |

**Remark**  $V_{PSI}$ : PSI pin reverse voltage

The S-8255B Series is initialized and the power-saving function is released by deactivating the PSI pin. As a result, each detection operation is carried out after returning to the normal status.

## 9. Temperature detection

Serially connect an NTC and a low temperature-dependent resistor ( $R_{TH}$ ) between the VDD pin and the VREG pin, and then connect their middle point to the TH pin. It allows for temperature detection at four different points: high temperature detection during charging, low temperature detection during charging, high temperature detection during discharging, low temperature detection during discharging.

When the temperature rises, according to the NTC temperature characteristics, the resistance ( $R_{NTC}$ ) decreases, and the ratio between  $R_{NTC}$  and  $R_{TH}$  changes, and then the TH pin voltage ( $V_{TH}$ ) increases.

When the temperature falls, according to the NTC temperature characteristics, the resistance ( $R_{NTC}$ ) increases, and the ratio between  $R_{NTC}$  and  $R_{TH}$  changes, and then the TH pin voltage ( $V_{TH}$ ) decreases.

The temperature detection during charging and temperature detection during discharging switch by comparing THC/DX pin voltage ( $V_{THC/DX}$ ) and either of THC/DX pin voltage "H" or "L" ( $V_{THH}$ ,  $V_{THL}$ ).

If the relation between  $R_{NTC}$ ,  $R_{TH}$ , and  $V_{THC/DX}$  satisfies the itemized condition in **Table 13** in each temperature detection, and each status continues for the temperature detection delay time ( $t_{TH}$ ) or longer, the CO pin changes to the  $V_{SS}$  level and the DO pin changes to the "H" or  $V_{SS}$  level. This is the temperature protection status.

If the itemized condition in **Table 13** is not satisfied in each temperature detection, and each status continues for  $t_{TH}$  or longer, the temperature protection status is released.

**Table 13 Conditions for Each Temperature Detection**

| Item  | TH Pin   | THC/DX Pin                | CO Pin         | DO Pin         |
|---|--|---------------------------|----------------|----------------|
| High temperature detection during charging    | $\Gamma_{THCH} \leq R_{TH} / (R_{NTC} + R_{TH})$ | $V_{THC/DX} \geq V_{THH}$ | $V_{SS}$ level | "H"            |
| Low temperature detection during charging     | $\Gamma_{THCL} \geq R_{TH} / (R_{NTC} + R_{TH})$ | $V_{THC/DX} \geq V_{THH}$ |                | $V_{SS}$ level |
| High temperature detection during discharging | $\Gamma_{THDH} \leq R_{TH} / (R_{NTC} + R_{TH})$ | $V_{THC/DX} \leq V_{THL}$ |                | $V_{SS}$ level |
| Low temperature detection during discharging  | $\Gamma_{THDL} \geq R_{TH} / (R_{NTC} + R_{TH})$ | $V_{THC/DX} \leq V_{THL}$ |                | $V_{SS}$ level |

**Remark**  $\Gamma_{THCH}$ : High temperature detection ratio during charging  
 $\Gamma_{THCL}$ : Low temperature detection ratio during charging  
 $\Gamma_{THDH}$ : High temperature detection ratio during discharging  
 $\Gamma_{THDL}$ : Low temperature detection ratio during discharging



The detection temperature can be set according to the NTC and  $R_{TH}$  characteristics.  
 For example, if  $R_{NTC}^*1$  and  $R_{TH}$  (10 k $\Omega$ ) are connected to S-8255BAA, each detection temperature is as follows.

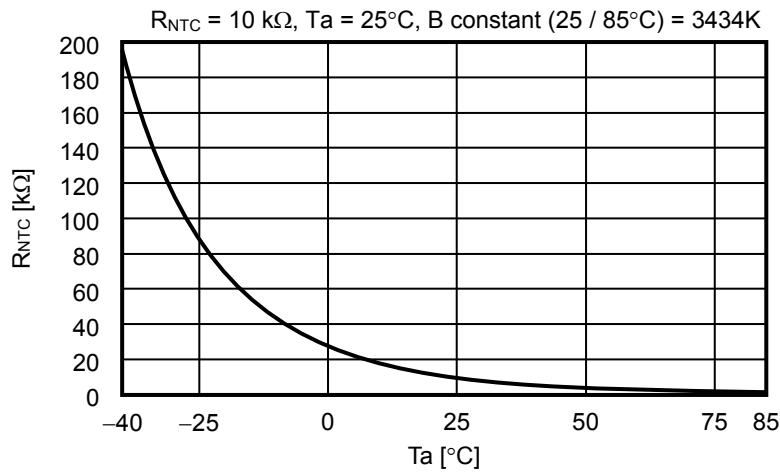
**Table 14**

| Item  | Temperature Detection Ratio | $R_{NTC}$       | Detection Temperature |
|---|-----------------------------|-----------------|-----------------------|
| Temperature for high temperature detection during charging    | $\Gamma_{THCH} = 0.670$     | 4.9 k $\Omega$  | 45°C                  |
| Temperature for low temperature detection during charging     | $\Gamma_{THCL} = 0.270$     | 27.0 k $\Omega$ | 0°C                   |
| Temperature for high temperature detection during discharging | $\Gamma_{THDH} = 0.795$     | 2.6 k $\Omega$  | 65°C                  |
| Temperature for low temperature detection during discharging  | $\Gamma_{THDL} = 0.190$     | 42.6 k $\Omega$ | -10°C                 |

\*1. The calculation method for  $R_{NTC}$  is as follows.

$$\begin{aligned} \Gamma_{THCL} &= R_{TH} / (R_{NTC} + R_{TH}) \\ R_{NTC} &= R_{TH} / \Gamma_{THCL} - R_{TH} \\ &= 10 \text{ k}\Omega / 0.270 - 10 \text{ k}\Omega \\ &= 27.0 \text{ k}\Omega \end{aligned}$$

When low temperature during charging is detected,  $R_{NTC} = 27.0 \text{ k}\Omega$ , so detection temperature = 0°C according to the  $R_{NTC}$  characteristics shown in **Figure 5**.

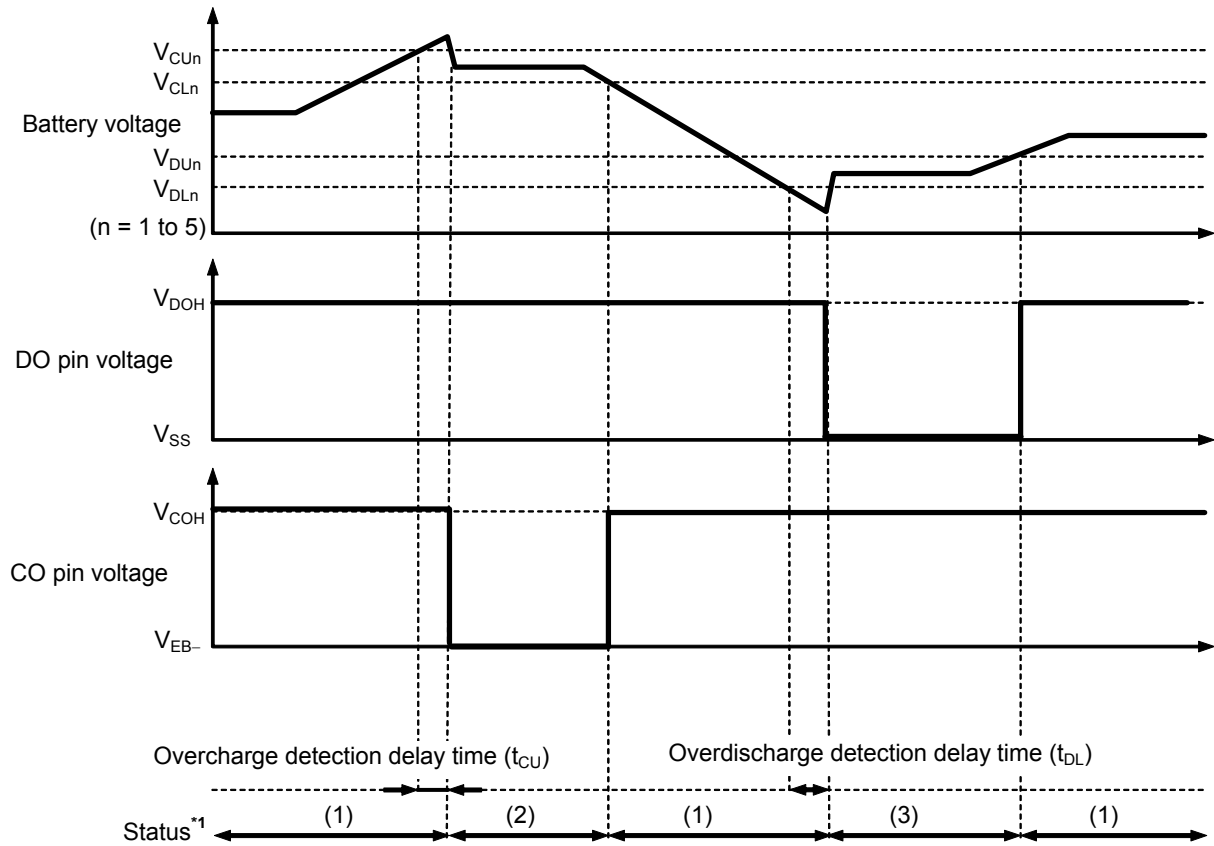


**Figure 5 Example of  $R_{NTC}$  Characteristics**

**Remark** Temperature detection is carried out intermittently for 512 ms typ. per cycle, of which 1 ms typ. is the detection operation period.  
 The VREG pin voltage is output only during detection operation. During other periods, the VREG pin is at the  $V_{DD}$  level.  
 Regarding details of intermittent operation, refer to "2. Temperature detection (High temperature detection during charging)" in "■ Timing Charts".

■ **Timing Charts**

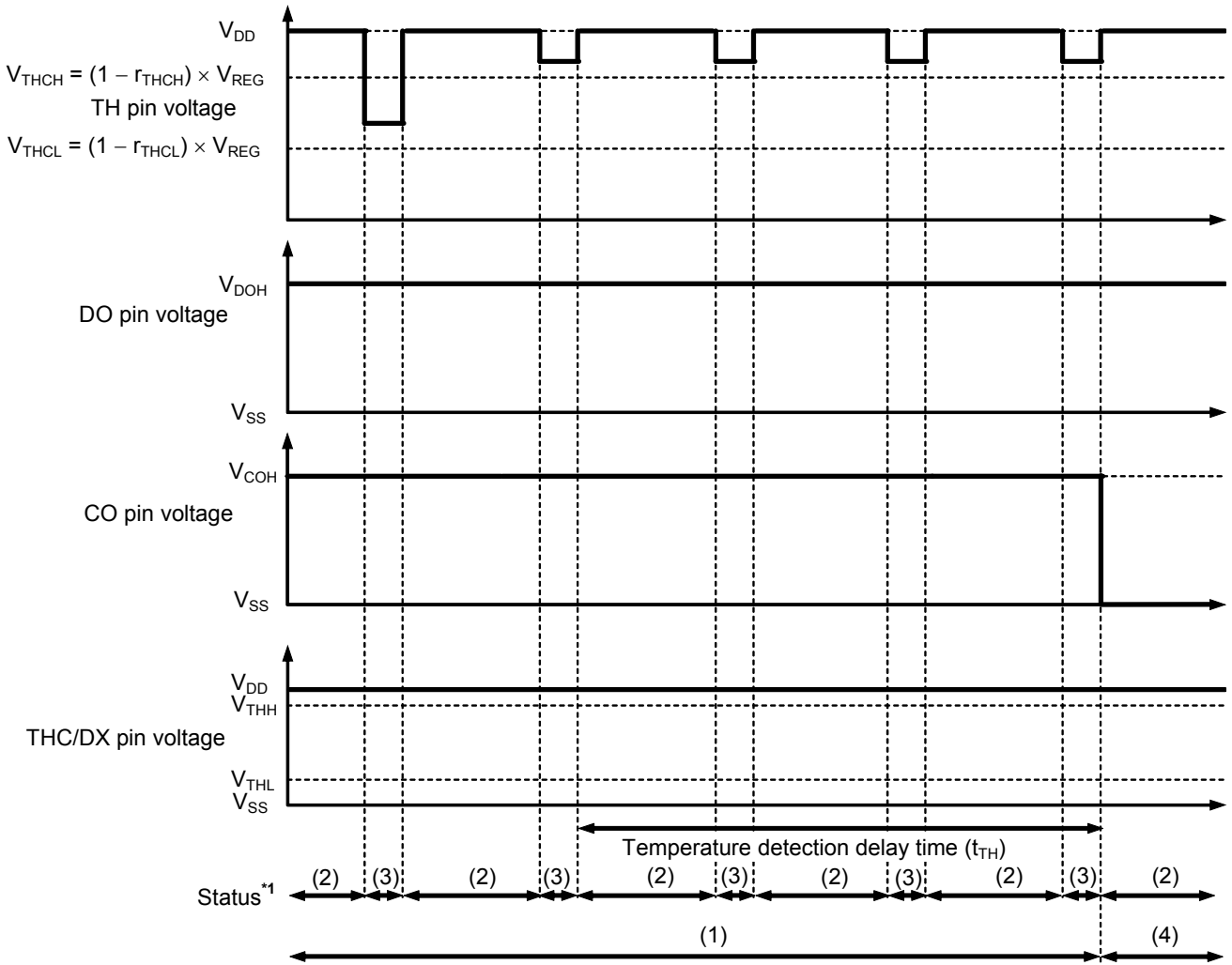
1. **Overcharge detection, overdischarge detection**



- \*1. (1) : Normal status  
 (2) : Overcharge status  
 (3) : Overdischarge status

Figure 6

2. Temperature detection (High temperature detection during charging)

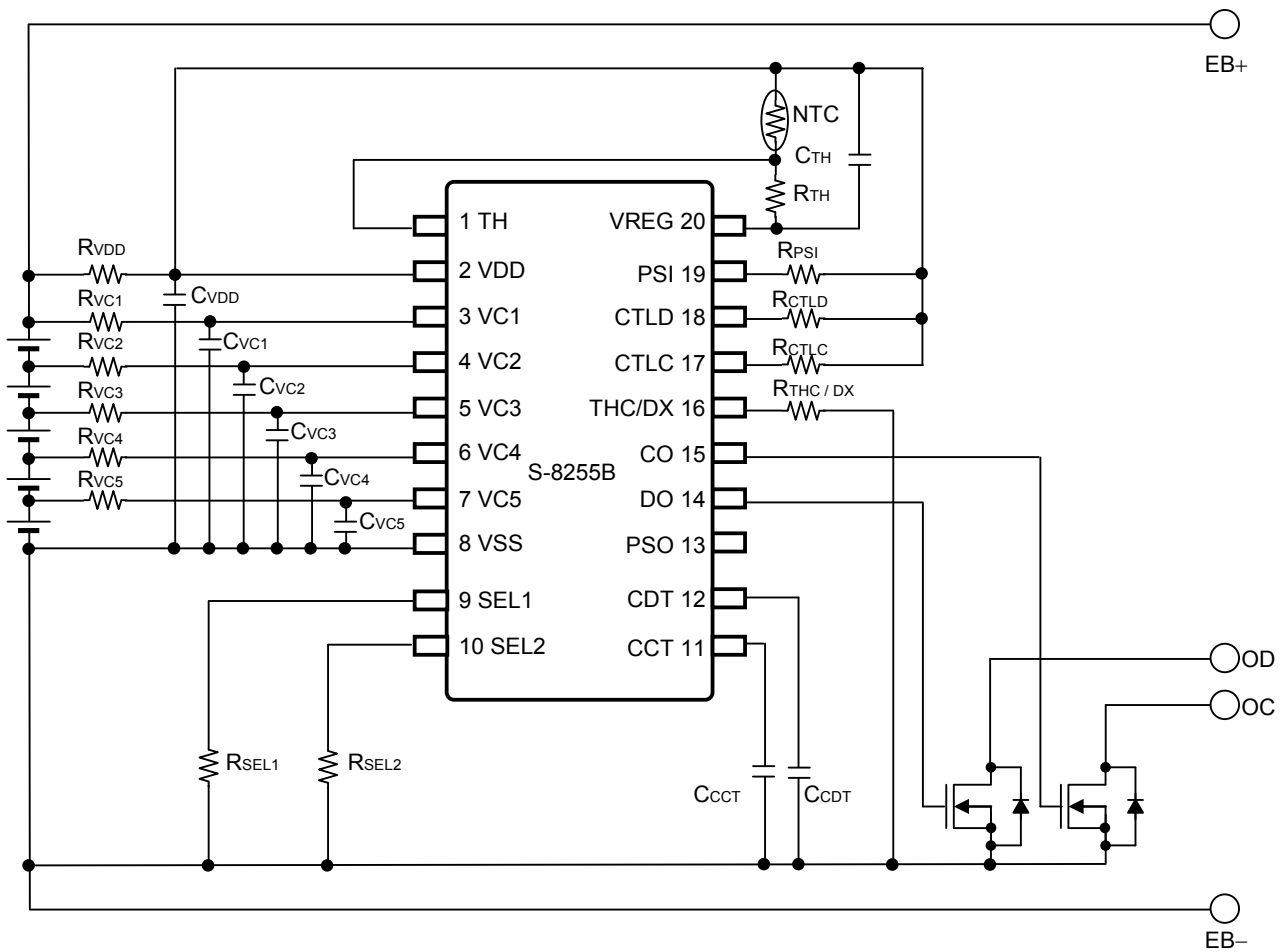


- \*1. (1) : Normal status
- (2) : Temperature detection sleep time
- (3) : Temperature detection awake time
- (4) : Temperature protection status

Figure 7

■ **Connection Examples of Battery Monitoring IC**

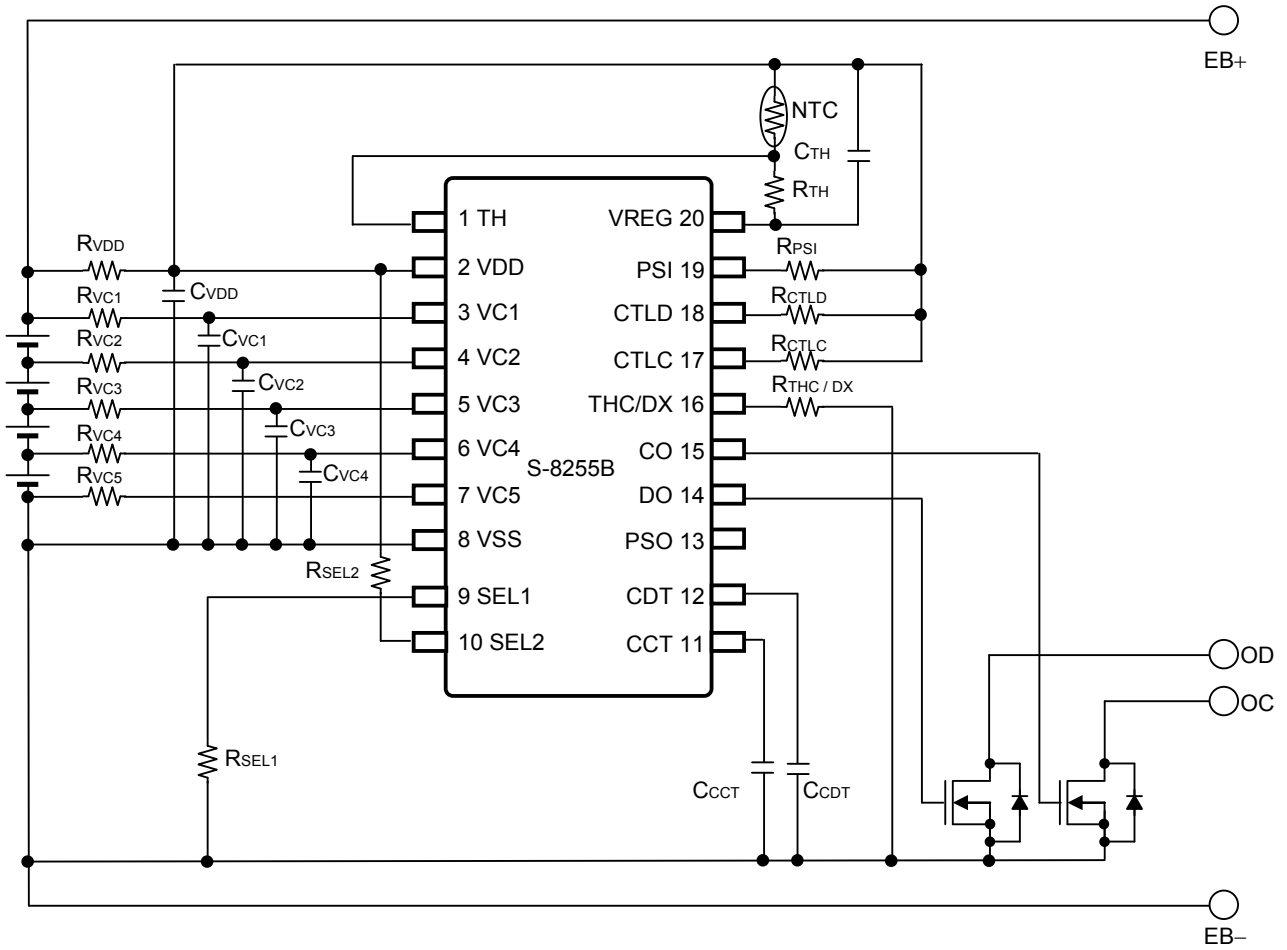
1. **S-8255B Series (5-serial cell)**



**Remark** Regarding the recommended values for external components, refer to "Table 15 Constants for External Components".

Figure 8

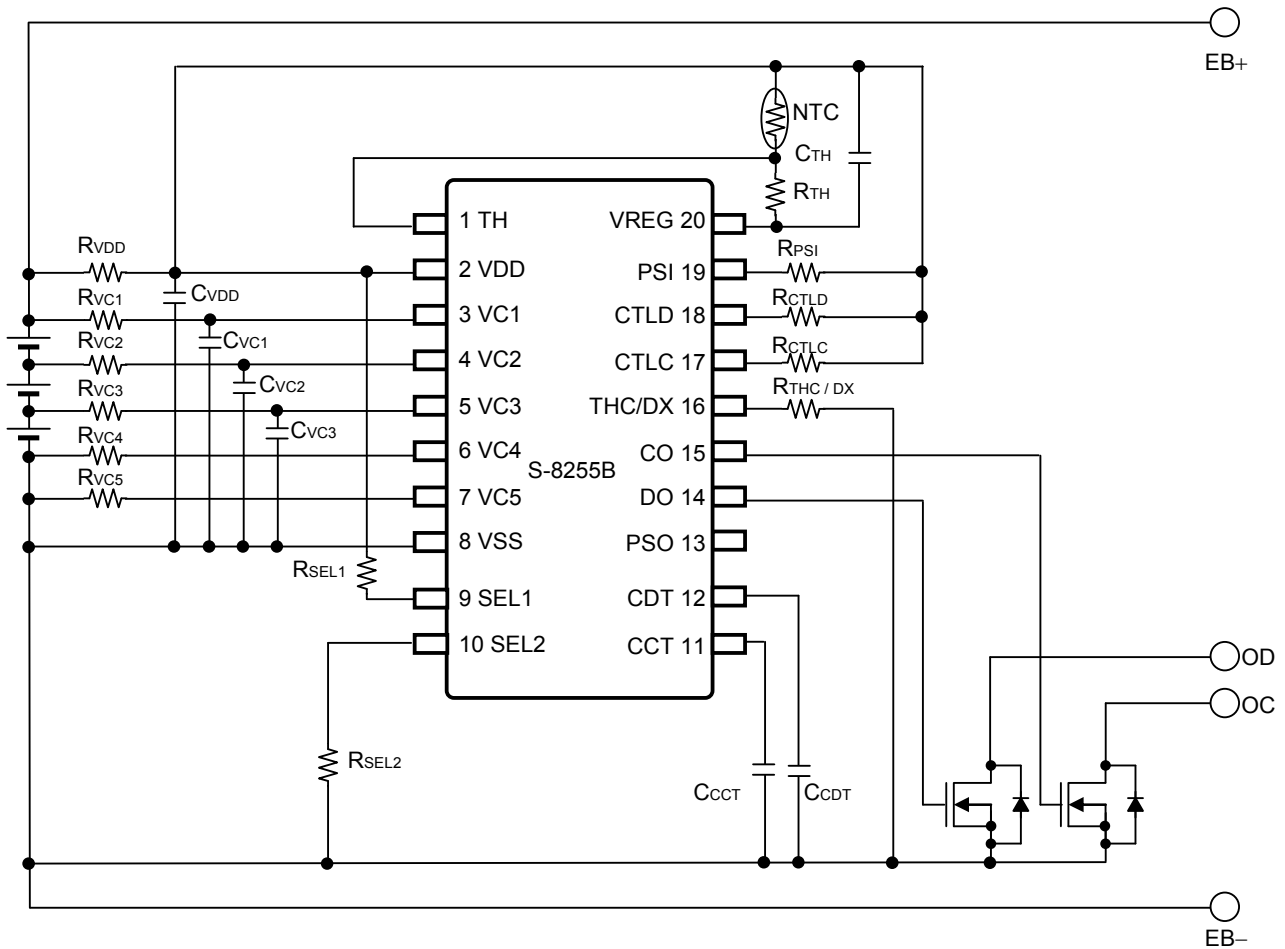
**2. S-8255B Series (4-serial cell)**



**Remark** Regarding the recommended values for external components, refer to "Table 15 Constants for External Components".

**Figure 9**

**3. S-8255B Series (3-serial cell)**



**Remark** Regarding the recommended values for external components, refer to "Table 15 Constants for External Components".

**Figure 10**

Table 15 Constants for External Components

| Symbol                               | Min.  | Typ.  | Max.  | Unit      |
|--------------------------------------|-------|-------|-------|-----------|
| $R_{VDD}^{*1}$                       | 68    | 100   | 100   | $\Omega$  |
| $R_{VCn} (n = 1 \text{ to } 5)^{*1}$ | 0.68  | 1.00  | 1.00  | $k\Omega$ |
| $R_{SEL1}, R_{SEL2}$                 | 1     | 1     | –     | $k\Omega$ |
| $R_{THC/DX}$                         | 1.0   | 1.0   | –     | $k\Omega$ |
| NTC                                  | –     | 10    | –     | $k\Omega$ |
| $R_{TH}$                             | –     | 10    | –     | $k\Omega$ |
| $C_{VDD}^{*1}$                       | 0.68  | 1.00  | 10.00 | $\mu F$   |
| $C_{VCn} (n = 1 \text{ to } 5)^{*1}$ | 0.068 | 0.100 | 1.000 | $\mu F$   |
| $C_{CCT}$                            | 0.01  | 0.10  | –     | $\mu F$   |
| $C_{CDT}$                            | 0.01  | 0.10  | –     | $\mu F$   |
| $C_{TH}$                             | 0.1   | 0.1   | 0.1   | $\mu F$   |

\*1.  $R_{VDD} \times C_{VDD} = 100 \mu F \cdot \Omega$  is recommended.

Set filter constants to satisfy  $R_{VC1} \times C_{VC1} = R_{VC2} \times C_{VC2} = R_{VC3} \times C_{VC3} = R_{VC4} \times C_{VC4} = R_{VC5} \times C_{VC5} = R_{VDD} \times C_{VDD}$ .

- Caution 1.** The above constants may be changed without notice.
- Sufficient evaluation of transient power supply fluctuation and overcurrent protection function with the actual application is needed to determine the proper constants when setting the filter constants between the VDD pin and VSS pin. Contact our sales office if setting the constants between the VDD pin and VSS pin to anything other than the recommended values.
  - It has not been confirmed whether the operation is normal or not in circuits other than the connection examples. In addition, the connection examples and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.

## ■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the power dissipation.
- Batteries can be connected in any order; however, there may be cases when discharging cannot be performed after a battery is connected. In this case, the S-8255B Series returns to the normal status when the following condition is satisfied.
  - Changing the PSI pin voltage to be  $V_{DS} \rightarrow 0\text{ V} \rightarrow V_{DS}$

**Remark**  $V_{DS}$ : Input voltage between VDD pin and VSS pin ( $V1 + V2 + V3 + V4 + V5$ )

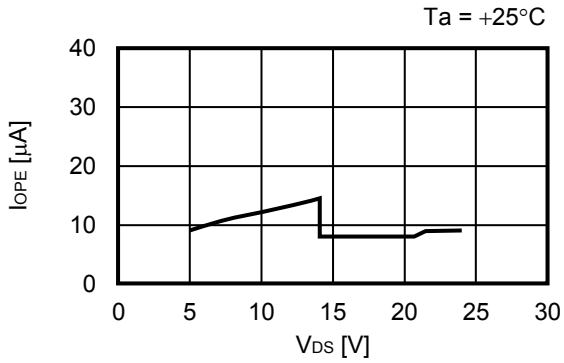
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.



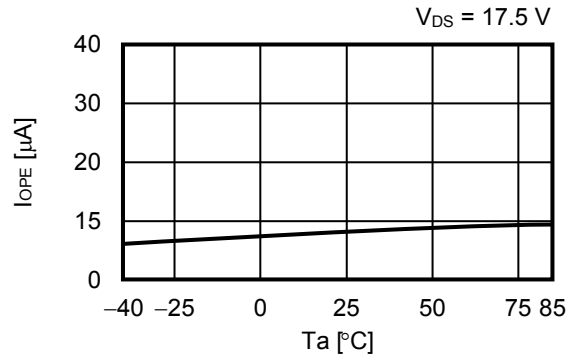
■ **Characteristics (Typical Data)**

**1. Current consumption**

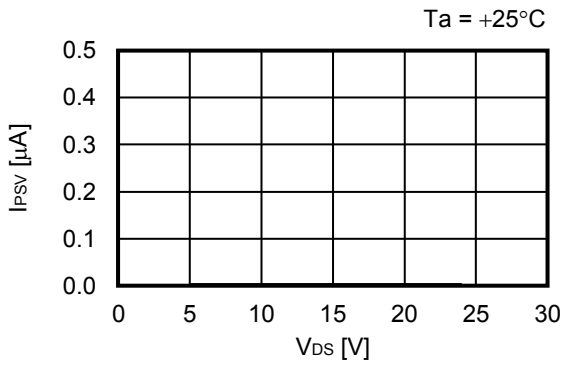
**1.1  $I_{OPE}$  vs.  $V_{DS}$**



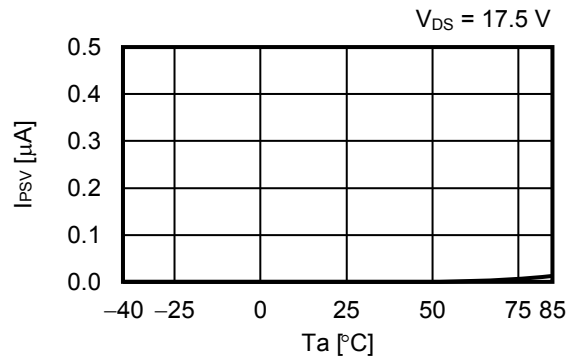
**1.2  $I_{OPE}$  vs.  $T_a$**



**1.3  $I_{PSV}$  vs.  $V_{DS}$**

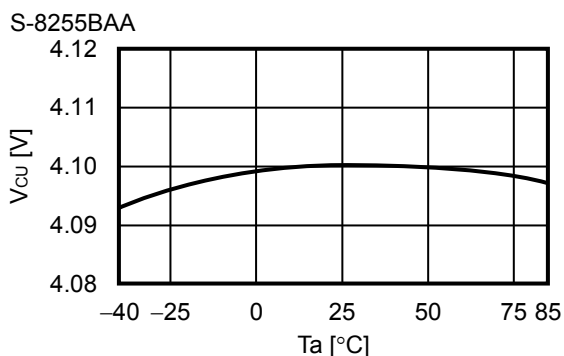


**1.4  $I_{PSV}$  vs.  $T_a$**

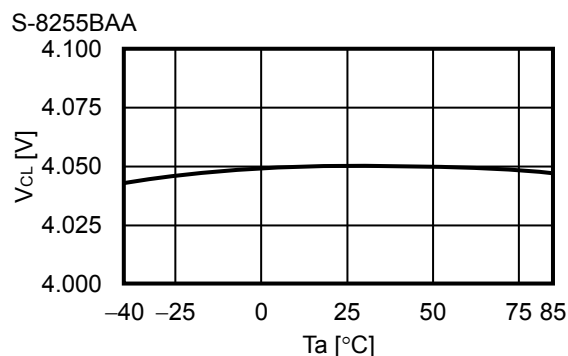


**2. Detection voltage, release voltage**

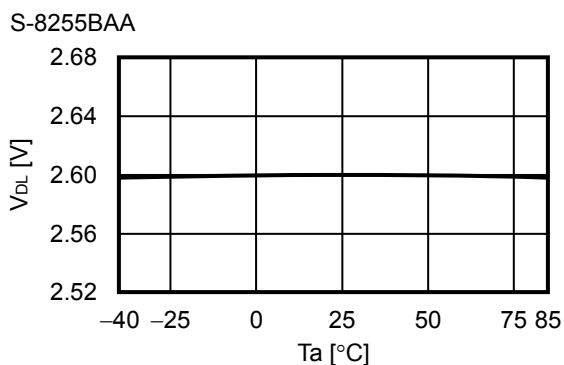
**2.1  $V_{CU}$  vs.  $T_a$**



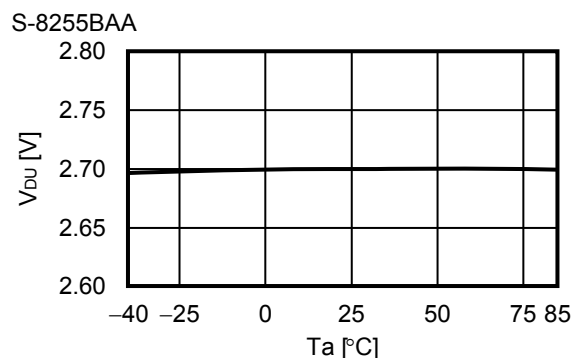
**2.2  $V_{CL}$  vs.  $T_a$**



**2.3  $V_{DL}$  vs.  $T_a$**

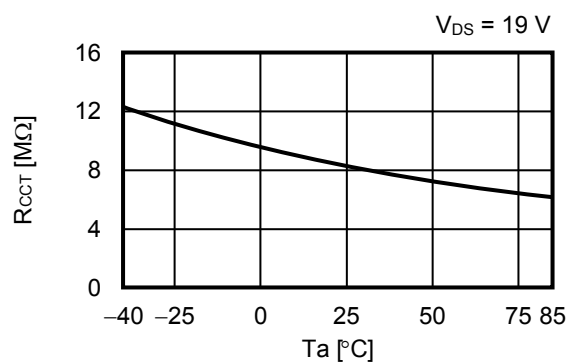


**2.4  $V_{DU}$  vs.  $T_a$**

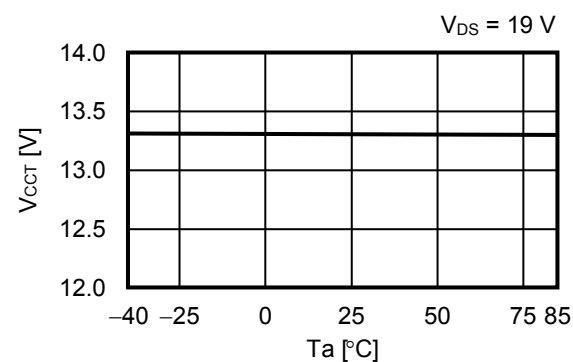


**3. Delay time function**

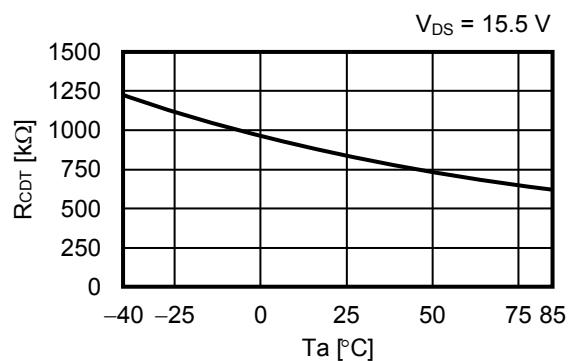
**3.1  $R_{CCT}$  vs.  $T_a$**



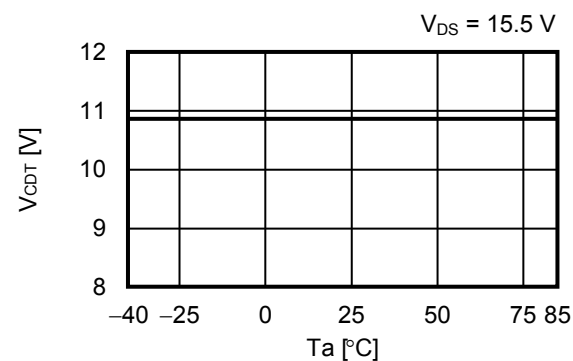
**3.2  $V_{CCT}$  vs.  $T_a$**



**3.3  $R_{CDT}$  vs.  $T_a$**

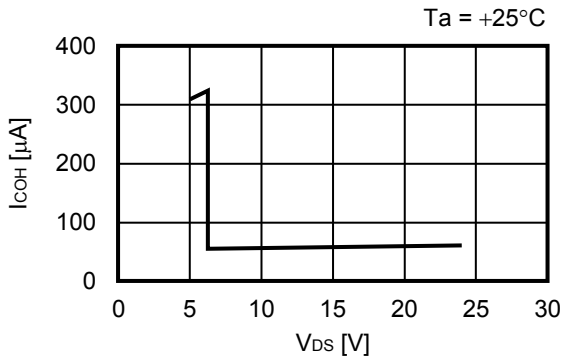


**3.4  $V_{CDT}$  vs.  $T_a$**

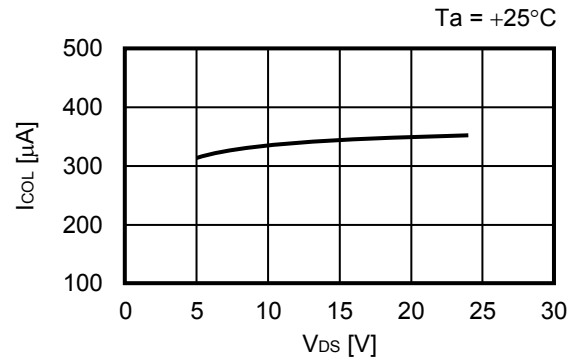


**4. Output pin**

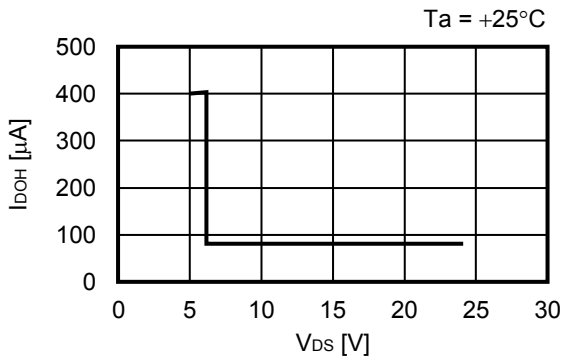
**4.1  $I_{COH}$  vs.  $V_{DS}$**



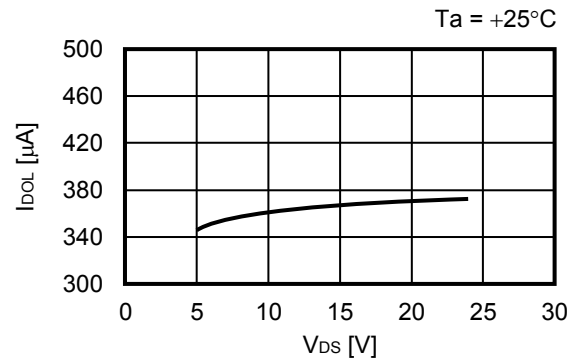
**4.2  $I_{COL}$  vs.  $V_{DS}$**



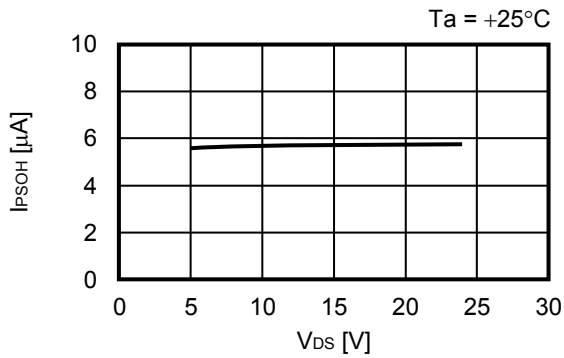
**4.3  $I_{DOH}$  vs.  $V_{DS}$**



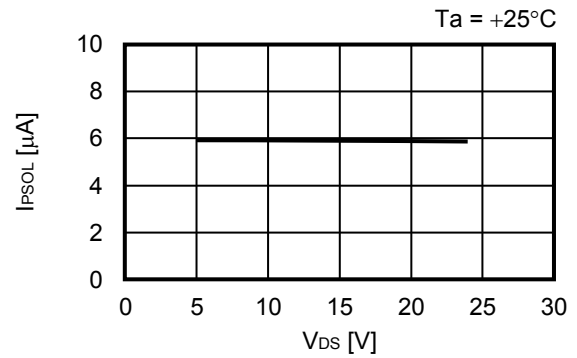
**4.4  $I_{DOL}$  vs.  $V_{DS}$**



**4.5  $I_{PSOH}$  vs.  $V_{DS}$**

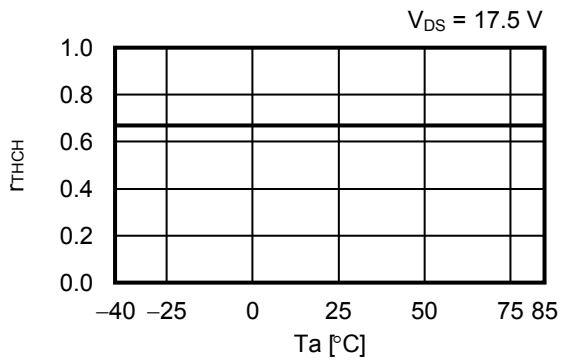


**4.6  $I_{PSOL}$  vs.  $V_{DS}$**

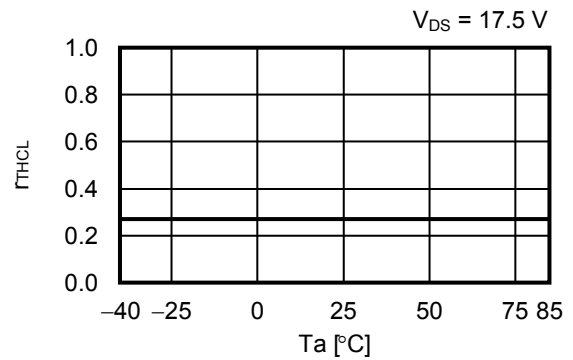


**5. Temperature detection function**

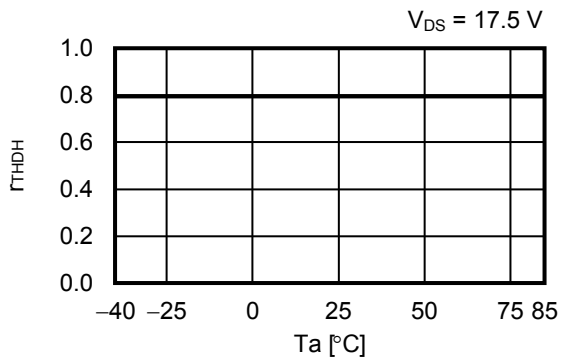
**5.1  $r_{THCH}$  vs.  $T_a$**



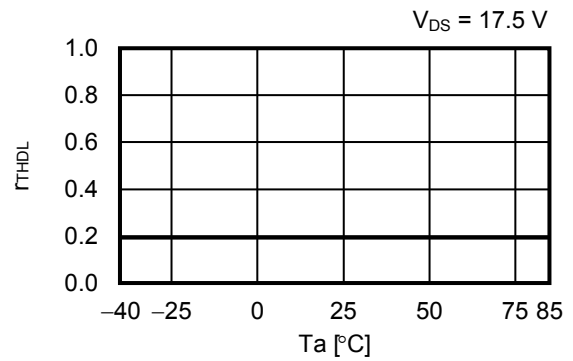
**5.2  $r_{THCL}$  vs.  $T_a$**



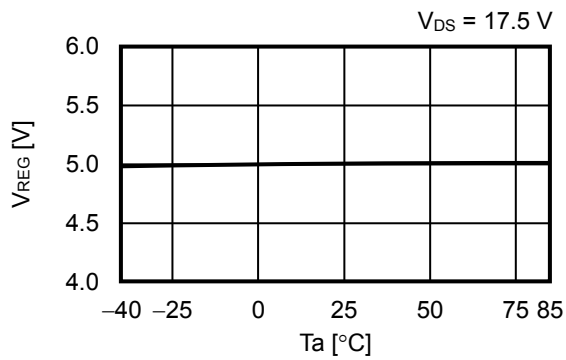
**5.3  $r_{THDH}$  vs.  $T_a$**



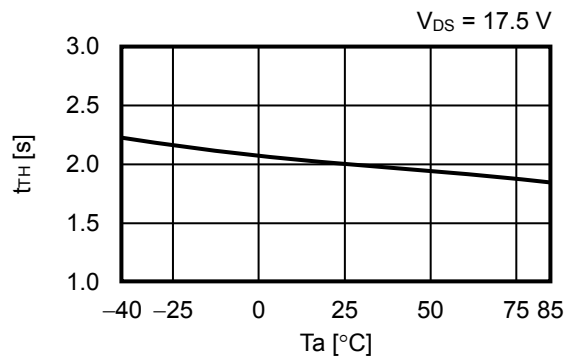
**5.4  $r_{THDL}$  vs.  $T_a$**



**5.5  $V_{REG}$  vs.  $T_a$**

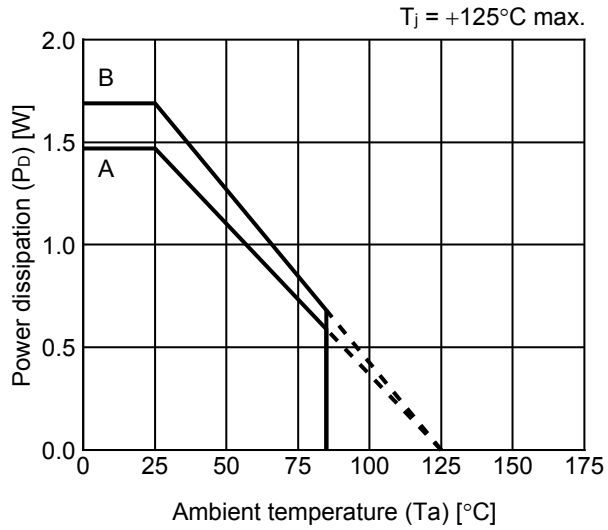


**5.6  $t_{TH}$  vs.  $T_a$**



■ **Power Dissipation**

**20-Pin TSSOP**

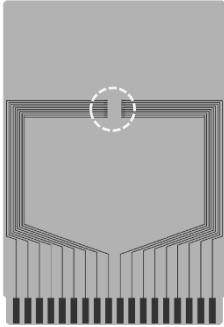


| Board | Power Dissipation ( $P_D$ ) |
|-------|-----------------------------|
| A     | 1.47 W                      |
| B     | 1.69 W                      |
| C     | -                           |
| D     | -                           |
| E     | -                           |

# 20-Pin TSSOP Test Board

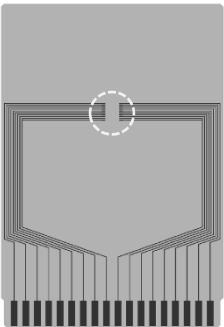
 IC Mount Area

(1) Board A



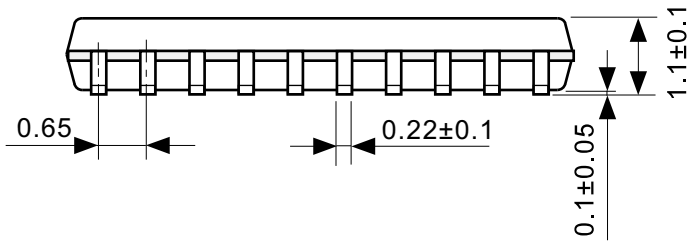
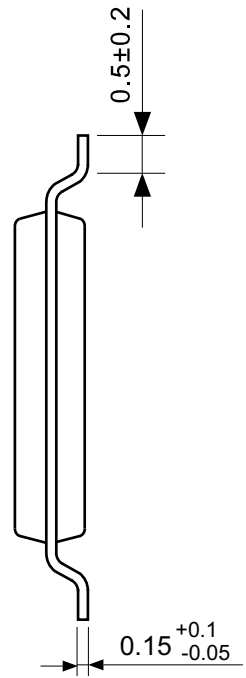
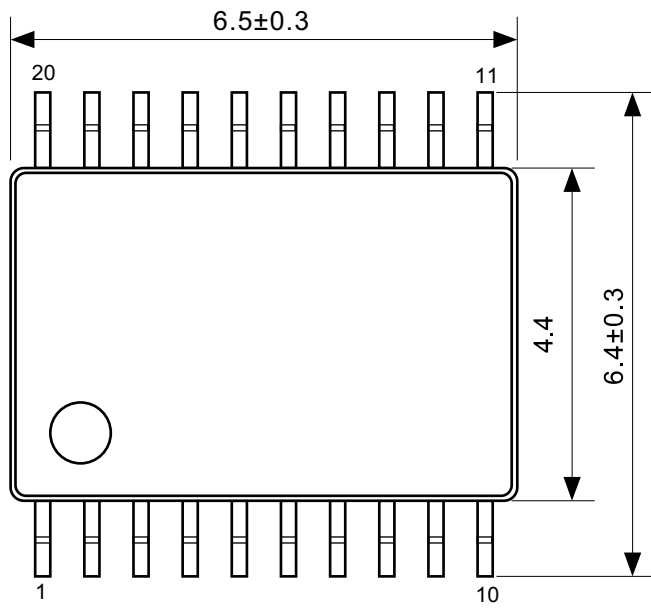
| Item                        |   | Specification                               |
|-----------------------------|---|---|
| Size [mm]                   |   | 114.3 x 76.2 x t1.6                         |
| Material                    |   | FR-4  |
| Number of copper foil layer |   | 2   |
| Copper foil layer [mm]      | 1 | Land pattern and wiring for testing: t0.070 |
|                             | 2 | -   |
|                             | 3 | -   |
|                             | 4 | 74.2 x 74.2 x t0.070                        |
| Thermal via                 |   | -   |

(2) Board B




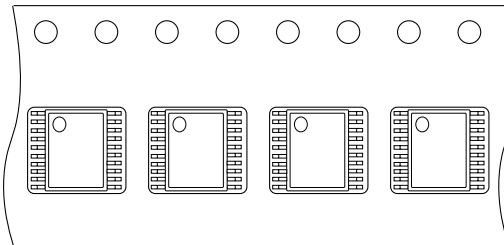
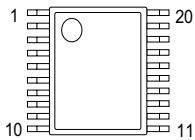
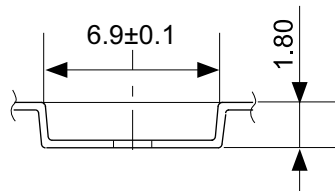
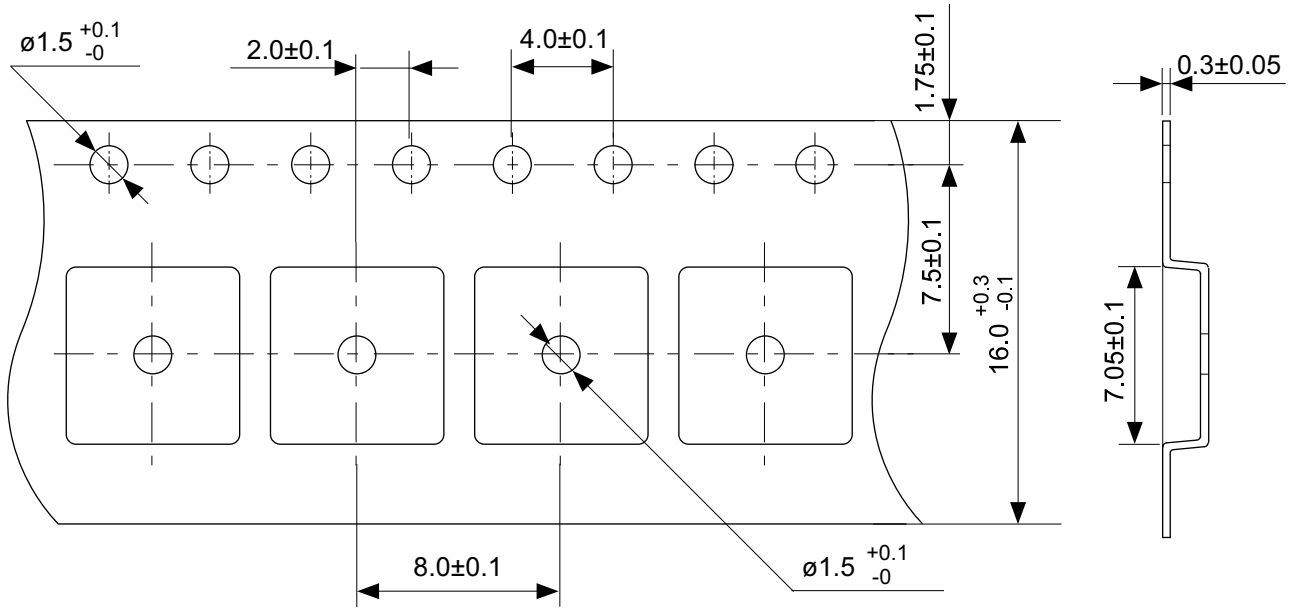
| Item                        |   | Specification                               |
|-----------------------------|---|---|
| Size [mm]                   |   | 114.3 x 76.2 x t1.6                         |
| Material                    |   | FR-4  |
| Number of copper foil layer |   | 4   |
| Copper foil layer [mm]      | 1 | Land pattern and wiring for testing: t0.070 |
|                             | 2 | 74.2 x 74.2 x t0.035                        |
|                             | 3 | 74.2 x 74.2 x t0.035                        |
|                             | 4 | 74.2 x 74.2 x t0.070                        |
| Thermal via                 |   | -   |

No. TSSOP20-A-Board-SD-1.0



No. FT020-B-P-SD-1.0

|                   |   |
|-------------------|---|
| TITLE             | TSSOP20-B-PKG Dimensions  |
| No.               | FT020-B-P-SD-1.0  |
| ANGLE             |  |
| UNIT              | mm  |
| <b>ABLIC Inc.</b> |   |

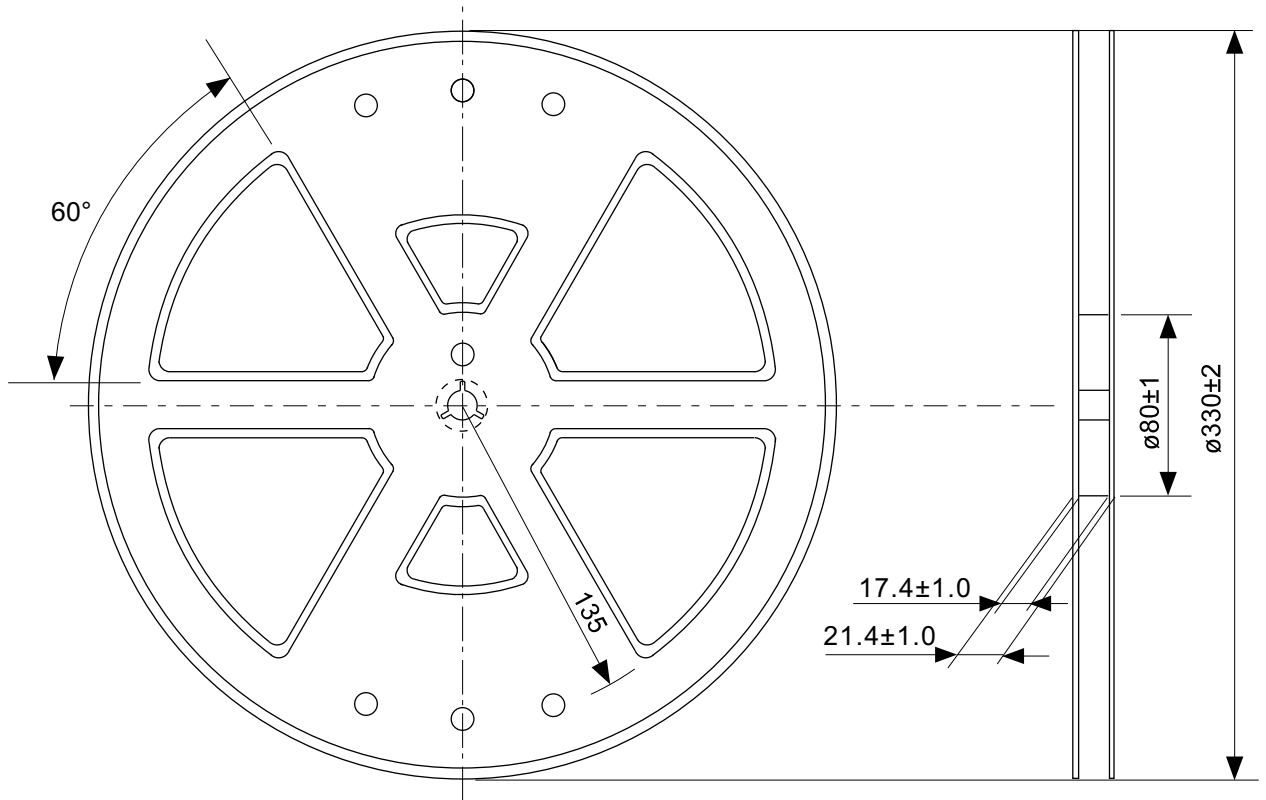


→  
Feed direction

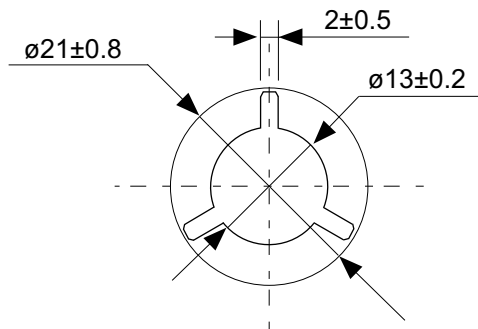
**No. FT020-B-C-SD-1.0**

|                   |                        |
|-------------------|------------------------|
| TITLE             | TSSOP20-B-Carrier Tape |
| No.               | FT020-B-C-SD-1.0       |
| ANGLE             |                        |
| UNIT              | mm                     |
| <b>ABLIC Inc.</b> |                        |





Enlarged drawing in the central part



No. FT020-B-R-SD-1.0

|                   |                  |      |       |
|-------------------|------------------|------|-------|
| TITLE             | TSSOP20-B-Reel   |      |       |
| No.               | FT020-B-R-SD-1.0 |      |       |
| ANGLE             |                  | QTY. | 4.000 |
| UNIT              | mm               |      |       |
|                   |                  |      |       |
| <b>ABLIC Inc.</b> |                  |      |       |

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2.4-2019.07