S-19193 Series

AUTOMOTIVE, 125°C OPERATION, BATTERY MONITORING IC FOR 3-SERIAL TO 6-SERIAL CELL PACK

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Rev.1.2_00

This IC is a monitoring IC for automotive rechargeable batteries, which includes high-accuracy voltage detection circuits and delay circuits. Switching control for 3-serial to 6-serial cell is possible by inputting voltage to the SEL1 pin and the SEL2 pin. By cascade connection, it is possible to protect 7-serial or more cells lithium-ion rechargeable battery pack. In addition, this IC can perform a self-test to confirm overcharge and overdischarge detection operations.

Caution This product can be used in vehicle equipment and in-vehicle equipment. Before using the product for these purposes, it is imperative to contact our sales representatives.

■ Features

- High-accuracy voltage detection circuit for each cell

Overcharge detection voltage n:	2.500 V to 4.500 V (25 mV step)	Accuracy ±20 mV (Ta = +25°C)
		Accuracy ±30 mV (Ta = –5°C to +55°C)
Overcharge release voltage n:	2.300 V to 4.500 V[*1]	Accuracy ±50 mV
Overdischarge detection voltage n:	1.000 V to 3.000 V (100 mV step)[*2]	Accuracy ±80 mV
Overdischarge release voltage n:	1.000 V to 3.300 V[*3]	Accuracy ±100 mV

- Self-test results to confirm overcharge and overdischarge detection operations can be output from the OUT1 pin and the OUT2 pin.
- Cascade connection function: Battery voltage monitoring of multiple modules is possible by connecting the upper module output to the CASI1 pin and the CASI2 pin.
- Each delay time is settable by an internal circuit only (External capacitors are not necessary).[*4]
  - Detection delay time: 0.5 ms, 1 ms, 2 ms, 4 ms, 8 ms, 16 ms, 32 ms, 64 ms, 128 ms, 256 ms
  - Release delay time: 0.25 ms, 0.5 ms, 1 ms, 2 ms, 4 ms, 8 ms, 16 ms
- Switching control for 3-serial to 6-serial cell is possible by inputting voltage to the SEL1 pin and the SEL2 pin.
- Two detection signal types:
  - Common: OUT1 pin: Overcharge and overdischarge detection signal
    OUT2 pin: Overcharge detection signal
  - Separate: OUT1 pin: Overcharge detection signal
    OUT2 pin: Overdischarge detection signal
- OUT1 pin, OUT2 pin output form: CMOS output
- OUT1 pin, OUT2 pin output logic: Active "H"
- High-withstand voltage: Absolute maximum rating 28.0 V
- Wide operation voltage range: 4.8 V to 28.0 V
- Wide operation temperature range: Ta = –40°C to +125°C
- Low current consumption
  - During operation: 20 μA max. (Ta = +25°C)
- Lead-free (Sn 100%), halogen-free
- AEC-Q100 in process[*5]
- This IC has been developed for the battery management system in accordance with ISO 26262. ABLIC Inc. can provide a safety manual for this IC.[*5, *6]

***1.** Overcharge release voltage = Overcharge detection voltage – Overcharge hysteresis voltage
(Overcharge hysteresis voltage n is selectable from 0 V to 400 mV in 50 mV step.)

***2.** When this IC is used for monitoring a 3-serial-cell battery, set the overdischarge detection voltage n to 1.6 V or higher.

***3.** Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage
(Overdischarge hysteresis voltage n is selectable from 0 V to 0.7 V in 100 mV step.)

***4.** Set the delay time to detection delay time > release delay time.

***5.** Contact our sales representatives for details.

***6.** A Non-Disclosure Agreement is necessary when providing the documents.

Remark n = 1 to 6

■ Application

- Automotive rechargeable battery pack (EV, HEV, PHEV, etc.)

■ Package

- HTSSOP-16

■ Block Diagram

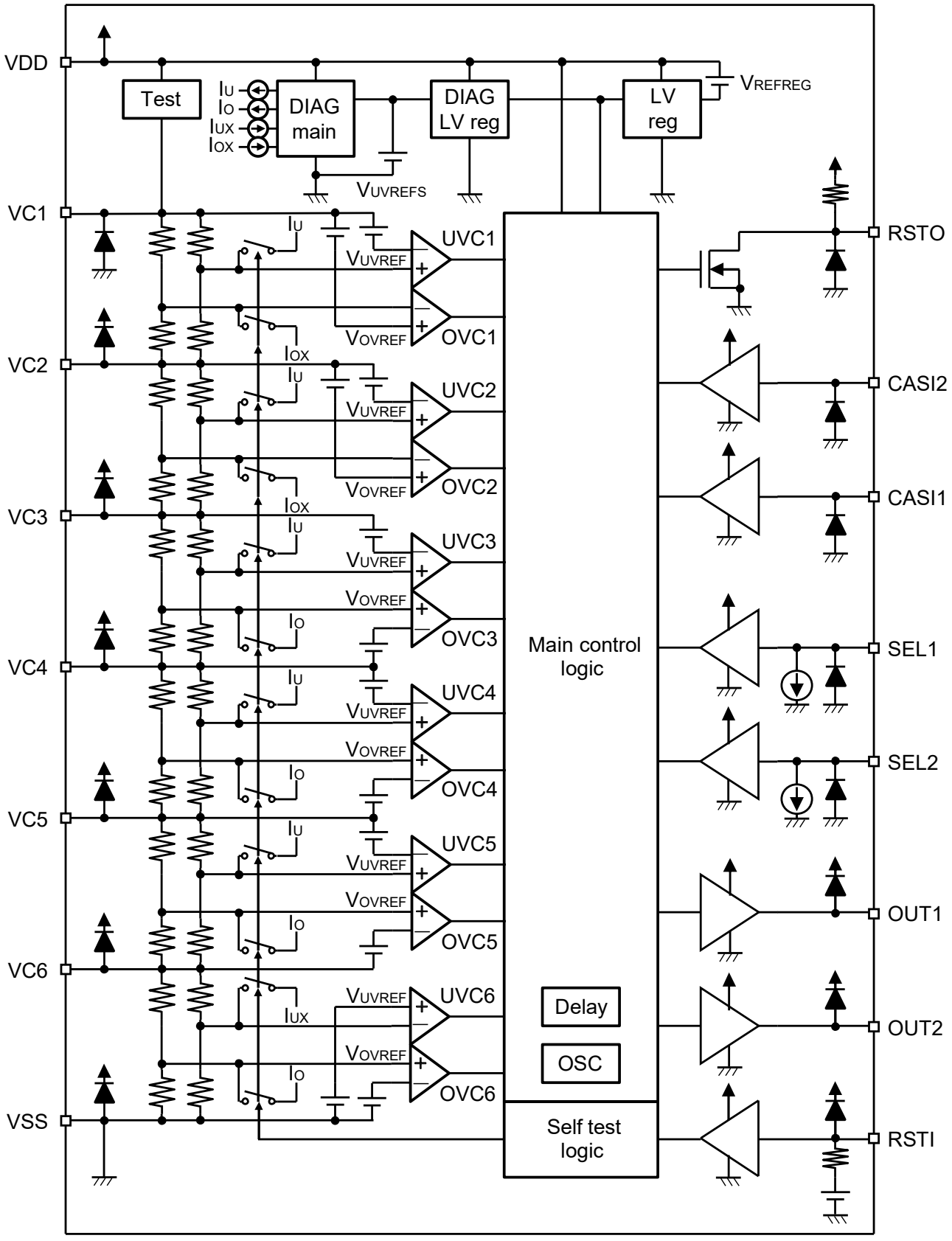


Figure 1

Remark The diodes in the figure are parasitic diodes.

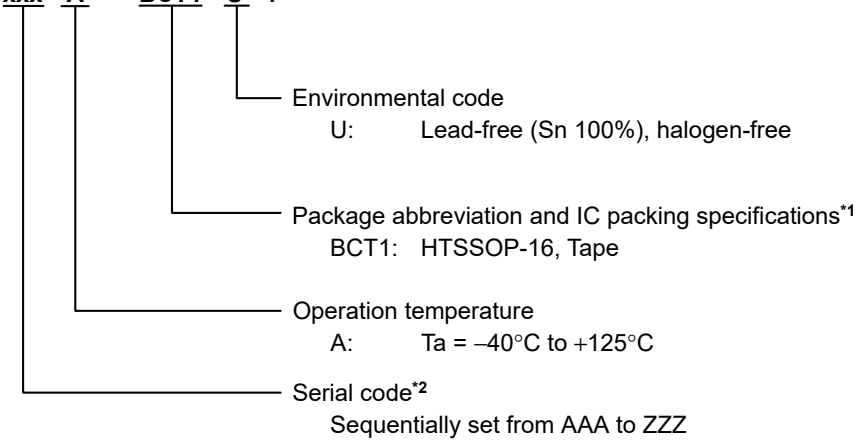
■ AEC-Q100 in Process

Contact our sales representatives for details of AEC-Q100 reliability specification.

■ Product Name Structure

1. Product name

S-19193 xxx A - BCT1 U 7



***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
HTSSOP-16	FR016-A-P-SD	FR016-A-C-SD	FR016-A-R-SD	FR016-A-L-SD

3. Product name list

Table 2

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Overdischarge Detection Voltage [V_{DL}]	Overdischarge Release Voltage [V_{DU}]	Detection Delay Time*1 [t_{DET}]	Release Delay Time*2 [t_{REL}]	Detection Signal Type*3
S-19193AAAA-BCT1U7	4.350 V	4.100 V	2.000 V	2.400 V	128 ms	2 ms	Common
S-19193AABA-BCT1U7	4.250 V	4.000 V	2.700 V	3.000 V	256 ms	2 ms	Separate
S-19193AACA-BCT1U7	3.650 V	3.400 V	2.500 V	2.900 V	256 ms	2 ms	Separate
S-19193AAEA-BCT1U7	3.550 V	3.350 V	2.000 V	2.300 V	256 ms	2 ms	Common
S-19193AAFA-BCT1U7	2.800 V	2.600 V	1.800 V	2.200 V	128 ms	2 ms	Separate
S-19193AAGA-BCT1U7	3.100 V	2.800 V	1.000 V	1.200 V	128 ms	2 ms	Separate

***1.** Detection delay time: 0.5 ms, 1 ms, 2 ms, 4 ms, 8 ms, 16 ms, 32 ms, 64 ms, 128 ms, 256 ms
***2.** Release delay time: 0.25 ms, 0.5 ms, 1 ms, 2 ms, 4 ms, 8 ms, 16 ms
***3.** Refer to **Table 3** for details on detection signal type.

Remark Please contact our sales representatives for products other than the above.

Table 3

Detection Signal Type	Overcharge Detection Signal	Overdischarge Detection Signal
Common	OUT1 pin, OUT2 pin	OUT1 pin
Separate	OUT1 pin	OUT2 pin

■ Pin Configuration

1. HTSSOP-16

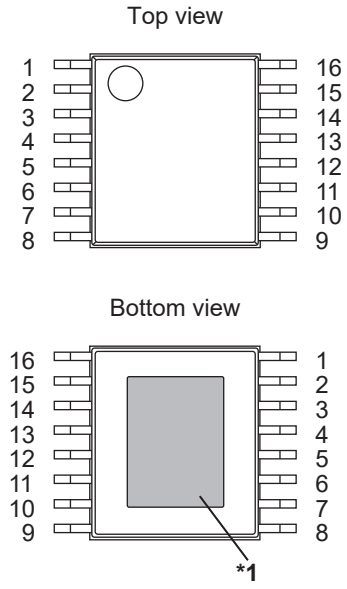


Figure 2

Table 4

Pin No.	Symbol	Description
1	VDD	Input pin for positive power supply, connection pin for positive voltage of battery 1
2	VC1	Connection pin for positive voltage of battery 1
3	VC2	Connection pin for negative voltage of battery 1, connection pin for positive voltage of battery 2
4	VC3	Connection pin for negative voltage of battery 2, connection pin for positive voltage of battery 3
5	VC4	Connection pin for negative voltage of battery 3, connection pin for positive voltage of battery 4
6	VC5	Connection pin for negative voltage of battery 4, connection pin for positive voltage of battery 5
7	VC6	Connection pin for negative voltage of battery 5, connection pin for positive voltage of battery 6
8	VSS	Input pin for negative power supply, connection pin for negative voltage of battery 6
9	RSTI	Input pin for reset signal
10	OUT2	Output pin 2 (Refer to "■ **Operation**" and "■ **Self-test Function**")
11	OUT1	Output pin 1 (Refer to "■ **Operation**" and "■ **Self-test Function**")
12	SEL2	Switching pins for number of serial cells [SEL1, SEL2] = ["High-Z", "High-Z"]: 6-serial cell [SEL1, SEL2] = ["High-Z", "H"]: 5-serial cell [SEL1, SEL2] = ["H", High-Z"]: 4-serial cell [SEL1, SEL2] = ["H", "H"]: 3-serial cell
13	SEL1	
14	CASI1	Input pin for cascade connection 1
15	CASI2	Input pin for cascade connection 2
16	RSTO	Output pin for reset signal

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential open.
Do not use it as the function of an electrode.

Remark High-Z: No connection

■ Absolute Maximum Ratings

Table 5

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin	V_{DS}	VDD	V_{SS} – 0.3 to V_{SS} + 28.0	V
Input pin voltage 1	V_{IN1}	VC1, VC2, VC3, VC4, VC5, VC6, SEL1, SEL2	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 28.0	V
Input pin voltage 2	V_{IN2}	CASI1, CASI2	V_{SS} – 0.3 to V_{DD} + 5.0 ≤ V_{SS} + 33.0	V
Input pin voltage 3	V_{IN3}	RSTI	V_{SS} – 5.0 to V_{DD} + 0.3 ≤ V_{SS} + 28.0	V
Output pin voltage 1	V_{OUT}	OUT1, OUT2	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 28.0	V
Output pin voltage 2	V_{RSTO}	RSTO	V_{SS} – 0.3 to V_{DD} + 5.0 ≤ V_{SS} + 33.0	V
Input pin current 1	I_{IN1}	CASI1, CASI2	150	μA
Input pin current 2	I_{IN2}	RSTI	–150	μA
Output pin current 1	I_{OUT}	OUT1, OUT2	–1.5	mA
Output pin current 2	I_{RSTO}	RSTO	1.5	mA
Operation ambient temperature	T_{opr}	–	–40 to +125	°C
Storage temperature	T_{stg}	–	–40 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 6

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	HTSSOP-16	Board A	–	91	–	°C/W
			Board B	–	65	–	°C/W
			Board C	–	34	–	°C/W
			Board D	–	32	–	°C/W
			Board E	–	26	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

Table 7 (1 / 2)

(V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, Ta = –40°C to +125°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Detection Voltage						
Overcharge detection voltage n	V_{CUn}	Ta = +25°C	V_{CUn} – 0.020	V_{CUn}	V_{CUn} + 0.020	V
		Ta = –5°C to +55°C	V_{CUn} – 0.030	V_{CUn}	V_{CUn} + 0.030	V
		–	V_{CUn} – 0.050	V_{CUn}	V_{CUn} + 0.050	V
Overdischarge detection voltage n	V_{DLn}	–	V_{DLn} – 0.080	V_{DLn}	V_{DLn} + 0.080	V
Release Voltage						
Overcharge release voltage n	V_{CLn}	–	V_{CLn} – 0.050	V_{CLn}	V_{CLn} + 0.050	V
Overdischarge release voltage n	V_{DUn}	–	V_{DUn} – 0.100	V_{DUn}	V_{DUn} + 0.100	V
Input Voltage						
Operation voltage between VDD pin and VSS pin	V_{DSOP}	–	4.8	–	28.0	V
SEL1 pin voltage "H"	V_{SEL1H}	–	V_{DS} – 0.5	–	–	V
SEL1 pin voltage "L"	V_{SEL1L}	–	–	–	0.3	V
SEL2 pin voltage "H"	V_{SEL2H}	–	V_{DS} – 0.5	–	–	V
SEL2 pin voltage "L"	V_{SEL2L}	–	–	–	0.3	V
RSTI pin voltage "H"	V_{RSTIH}	–	1.5	–	–	V
RSTI pin voltage "L"	V_{RSTIL}	–	–	–	0.4	V
CASI1 pin reverse voltage*1	V_{CASI1L}	Reverse voltage during isolated cascade connection	–	–	0.4	V
CASI2 pin reverse voltage*1	V_{CASI2L}	Reverse voltage during isolated cascade connection	–	–	0.4	V
CASI1 pin reverse voltage during communication*1	V_{CASI1C}	100 kΩ resistor connnected to the CASI1 pin, reverse voltage during cascade connection	V_{DS} + 0.5	–	V_{DS} + 2.4	V
CASI2 pin reverse voltage during communication*1	V_{CASI2C}	100 kΩ resistor connnected to the CASI2 pin, reverse voltage during cascade connection	V_{DS} + 0.5	–	V_{DS} + 2.4	V

***1.** Refer to "■ **Test Circuit**".

Remark n = 1 to 6

Table 7 (2 / 2)

(V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, Ta = –40°C to +125°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Current						
Current consumption during operation	I_{OPE}	–	–	10	20	µA
Current consumption during overcharge	I_{OPEC}	V1 = V2 = V3 = V4 = V5 = V6 = V_{CU} + 0.1 V	–	–	20	µA
Current consumption during overdischarge	I_{OPED}	V1 = V2 = V3 = V4 = V5 = V6 = V_{DL} – 0.1 V	–	–	20	µA
VC1 pin current	I_{VC1}	–	–	0.5	1.5	µA
VC2 pin current	I_{VC2}	–	–0.2	0.2	0.5	µA
VC3 pin current	I_{VC3}	–	–0.1	0.0	0.1	µA
VC4 pin current	I_{VC4}	–	–0.2	0.0	0.1	µA
VC5 pin current	I_{VC5}	–	–0.2	0.0	0.1	µA
VC6 pin current	I_{VC6}	–	–0.2	0.0	0.1	µA
SEL1 pin sink current	I_{SEL1H}	V_{SEL1} = V_{DS}	–	0.1	0.4	µA
SEL1 pin leakage current	I_{SEL1L}	V_{SEL1} = 0 V	–0.1	–	0.1	µA
SEL2 pin sink current	I_{SEL2H}	V_{SEL2} = V_{DS}	–	0.1	0.4	µA
SEL2 pin leakage current	I_{SEL2L}	V_{SEL2} = 0 V	–0.1	–	0.1	µA
RSTI pin sink current	I_{RSTIH}	V_{RSTI} = V_{DS}	0	0.1	0.5	µA
RSTI pin source current	I_{RSTIL}	V_{RSTI} = 0 V	–10.0	–1.8	–	µA
CASI1 pin sink current	I_{CASI1H}	V_{CASI1} = V_{DS}	–	0.1	1.0	µA
CASI1 pin source current	I_{CASI1L}	V_{CASI1} = 0 V	–10.0	–2.2	–	µA
CASI2 pin sink current	I_{CASI2H}	V_{CASI2} = V_{DS}	–	0.1	1.0	µA
CASI2 pin source current	I_{CASI2L}	V_{CASI2} = 0 V	–10.0	–2.2	–	µA
Output Voltage						
RSTI pin output voltage during no-load	V_{RSTIO}	I_{RSTO} = 0 µA	1.5	2.9	4.0	V
Output Current						
OUT1 pin, OUT2 pin output current						
OUT1 pin source current	I_{OUT1H}	V_{OUT1} = V_{DS} – 0.5 V	–	–	–200	µA
OUT1 pin sink current	I_{OUT1L}	V_{OUT1} = 0.5 V	2.0	–	–	µA
OUT2 pin source current	I_{OUT2H}	V_{OUT2} = V_{DS} – 0.5 V	–	–	–200	µA
OUT2 pin sink current	I_{OUT2L}	V_{OUT2} = 0.5 V	2.0	–	–	µA
RSTO pin leakage current	I_{RSTOH}	V_{RSTO} = V_{DS}	–0.1	–	0.1	µA
RSTO pin sink current	I_{RSTOL}	V_{RSTO} = 0.5 V	200	–	–	µA
Delay Time						
Detection delay time	t_{DET}	–	t_{DET} × 0.7 – 0.1	t_{DET}	t_{DET} × 1.3 + 0.2	ms
Release delay time	t_{REL}	–	t_{REL} × 0.7 – 0.1	t_{REL}	t_{REL} × 1.3 + 0.2	ms
Delay Time during Self-test						
Self-test start time	t_{STA}	–	5	10	15	ms
Diagnosis time	t_{DIAG}	–	46	66	86	ms
Overcharge diagnostic holding time	t_{DCHD}	–	1.2	2.0	2.8	ms
Overdischarge diagnostic holding time	t_{DDHD}	–	1.2	2.0	2.8	ms
Normal status holding time	t_{NMLD}	–	1.2	2.0	2.8	ms

■ Test Circuit

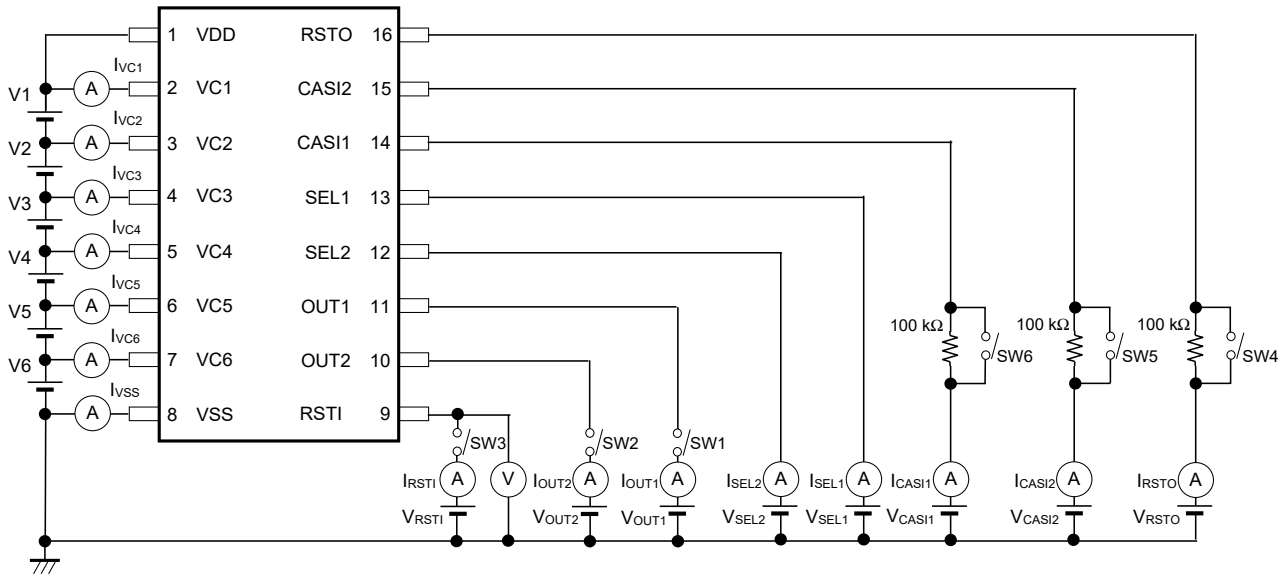


Figure 3

Remark Set SW1, SW2, SW3, SW4, SW5 and SW6 to OFF unless otherwise specified.

1. Overcharge detection voltage n (V_{CUn}), overcharge release voltage n (V_{CLn})

After setting V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{RSTI} = V_{CASI1} = V_{CASI2} = V_{DS} and V_{SEL1} = V_{SEL2} = 0 V, the voltage V1 is gradually increased. When the OUT1 pin output switches to the detection status, the voltage V1 is defined as V_{CU1}. The voltage V1 is then gradually decreased. When the OUT1 pin output switches to the release status, the voltage V1 is defined as V_{CL1}. Similarly, V_{CUn} and V_{CLn} can be defined by changing Vn (n = 2 to 6).

2. Overdischarge detection voltage n (V_{DLn}), overdischarge release voltage n (V_{DUn})

After setting V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{RSTI} = V_{CASI1} = V_{CASI2} = V_{DS}, and V_{SEL1} = V_{SEL2} = 0 V, the voltage V1 is gradually decreased. When the OUT1 pin output or OUT2 pin output*1 switches to the detection status, the voltage V1 is defined as V_{DL1}. The voltage V1 is then gradually increased. When the OUT1 pin output or OUT2 pin output*1 switches to the release status, the voltage V1 is defined as V_{DU1}. Similarly, V_{DLn} and V_{DUn} can be defined by changing Vn (n = 2 to 6).

***1.** When the detection signal type is "common", it is OUT1 pin output.
When the detection signal type is "separate", it is OUT2 pin output.

3. SEL1 pin voltage "H" (V_{SEL1H}), SEL1 pin voltage "L" (V_{SEL1L}), SEL2 pin voltage "H" (V_{SEL2H}), SEL2 pin voltage "L" (V_{SEL2L})

After setting V1 = V2 = V3 = V4 = V6 = V_{DU} + 0.1 V, V_{RSTI} = V_{CASI1} = V_{CASI2} = V_{DS}, V_{SEL1} = V_{SEL2} = 0 V, and V5 = V_{DL} − 0.1 V, the voltage V_{SEL1} is gradually increased. When the OUT1 pin output switches to the release status, the voltage V_{SEL1} is defined as V_{SEL1H}. The voltage V_{SEL1} is then gradually decreased. When the OUT1 pin output switches to the detection status, the voltage V_{SEL1} is defined as V_{SEL1L}. Similarly, V_{SEL2H} and V_{SEL2L} can be defined by changing V_{SEL2}.

4. RSTI pin voltage "H" (V_{RSTIH}), RSTI pin voltage "L" (V_{RSTIL})

After setting V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{RSTI} = V_{CASI1} = V_{CASI2} = V_{DS}, V_{SEL1} = V_{SEL2} = 0 V and SW3 = ON, V_{RSTI} is gradually decreased. When the self-test is performed, the voltage V_{RSTI} is defined as V_{RSTIL}. When the self-test is completed, the output voltage of the RSTO pin becomes "L". The V_{RSTI} is then gradually increased. When V_{RSTO} goes "H", the voltage V_{RSTI} is defined as V_{RSTIH}.

5. CASI1 pin reverse voltage (V_{CASI1L}), CASI2 pin reverse voltage (V_{CASI2L})

After setting V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{RSTI} = V_{CASI1} = V_{CASI2} = V_{DS}, V_{SEL1} = V_{SEL2} = 0 V, SW5 = ON and SW6 = ON, the voltage V_{CASI1} is gradually decreased. When the OUT1 pin output*1 switches to the detection status, the voltage V_{CASI1} is defined as V_{CASI1L}. Similarly, when the voltage V_{CASI2} is gradually decreased and the OUT2 pin output switches to the detection status, the voltage V_{CASI2} is defined as V_{CASI2L}.

6. CASI1 pin reverse voltage during communication (V_{CASI1C}), CASI2 pin reverse voltage during communication (V_{CASI2C})

After setting V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{RSTI} = V_{CASI1} = V_{CASI2} = V_{DS}, V_{SEL1} = V_{SEL2} = 0 V, SW5 = OFF and SW6 = OFF, the voltage V_{CASI1} is gradually increased. When the OUT1 pin output*1 switches to the detection status, the voltage V_{CASI1} is defined as V_{CASI1C}. Similarly, when the voltage V_{CASI2} is gradually increased and the OUT2 pin output switches to the detection status, the voltage V_{CASI2} is defined as V_{CASI2C}.

7. Current consumption during operation (I_{OPE}), current consumption during overcharge (I_{OPEC}), current consumption during overdischarge (I_{OPED})

When V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{RSTI} = V_{CASI1} = V_{CASI2} = V_{DS}, V_{SEL1} = V_{SEL2} = 0 V, SW1 = OFF and SW2 = OFF, the VSS pin current is defined as I_{OPE}.
When V1 = V2 = V3 = V4 = V5 = V6 = V_{CU} + 0.1 V, V_{RSTI} = V_{CASI1} = V_{CASI2} = V_{DS}, V_{SEL1} = V_{SEL2} = 0 V, SW1 = OFF and SW2 = OFF, the VSS pin current is defined as I_{OPEC}.
When V1 = V2 = V3 = V4 = V5 = V6 = V_{DL} − 0.1 V, V_{RSTI} = V_{CASI1} = V_{CASI2} = V_{DS}, V_{SEL1} = V_{SEL2} = 0 V, SW1 = OFF and SW2 = OFF, the VSS pin current is defined as I_{OPED}.

8. VCn pin current (I_{VCn}) (n = 1 to 6)

When V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{RSTI} = V_{CASI1} = V_{CASI2} = V_{DS} and V_{SEL1} = V_{SEL2} = 0 V, the VCn pin current is defined as I_{VCn}.

9. SEL1 pin sink current (I_{SEL1H}), SEL1 pin leakage current (I_{SEL1L}), SEL2 pin sink current (I_{SEL2H}), SEL2 pin leakage current (I_{SEL2L})

When V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{RSTI} = V_{CASI1} = V_{CASI2} = V_{DS} and V_{SEL1} = V_{SEL2} = 0 V, the SEL1 pin current and SEL2 pin current are defined as I_{SEL1L} and I_{SEL2L}, respectively.
When V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{RSTI} = V_{CASI1} = V_{CASI2} = V_{DS}, V_{SEL2} = 0 V and V_{SEL1} = V_{DS}, the SEL1 pin current is defined as I_{SEL1H}.
When V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{RSTI} = V_{CASI1} = V_{CASI2} = V_{DS}, V_{SEL1} = 0 V and V_{SEL2} = V_{DS}, the SEL2 pin current is defined as I_{SEL2H}.

10. RSTI pin sink current (I_{RSTIH}), RSTI pin source current (I_{RSTIL})

When V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{CASI1} = V_{CASI2} = V_{DS}, V_{SEL1} = V_{SEL2} = 0 V, V_{RSTI} = 0 V and SW3 = ON, the RSTI pin current is defined as I_{RSTIL}.
When V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{RSTI} = V_{CASI1} = V_{CASI2} = V_{DS}, V_{SEL1} = V_{SEL2} = 0 V and SW3 = ON, the RSTI pin current is defined as I_{RSTIH}.

11. CASI1 pin sink current (I_{CASI1H}), CASI1 pin source current (I_{CASI1L}), CASI2 pin sink current (I_{CASI2H}), CASI2 pin source current (I_{CASI2L})

When V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{RSTI} = V_{CASI1} = V_{CASI2} = V_{DS}, V_{SEL1} = V_{SEL2} = 0 V, SW5 = ON and SW6 = ON, the CASI1 pin current is defined as I_{CASI1L} and the CASI2 pin current is defined as I_{CASI2L}.
When V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{RSTI} = V_{CASI1} = V_{CASI2} = V_{SEL1} = V_{SEL2} = 0 V, SW5 = ON and SW6 = ON, the CASI1 pin current is defined as I_{CASI1H} and the CASI2 pin current is defined as I_{CASI2H}.

12. RSTI pin output voltage at no load (V_{RSTIO})

After setting V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{CASI1} = V_{CASI2} = V_{DS}, and V_{SEL1} = V_{SEL2} = 0 V, the output voltage of the RSTI pin is defined as V_{RSTIO} when SW3 is OFF.

13. OUT1 pin source current (I_{OUT1H}), OUT1 pin sink current (I_{OUT1L}), OUT2 pin source current (I_{OUT2H}), OUT2 pin sink current (I_{OUT2L})

When V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{RSTI} = V_{CASI1} = V_{CASI2} = V_{DS}, V_{SEL1} = V_{SEL2} = 0 V, V_{OUT1} = V_{OUT2} = 0.5 V, and SW1 = ON, the OUT1 pin current is I_{OUT1L}. Similarly, when SW2 = ON, the OUT2 pin current is I_{OUT2L}.
When V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{RSTI} = V_{DS}, V_{CASI1} = V_{CASI2} = V_{SEL1} = V_{SEL2} = 0 V, V_{OUT1} = V_{OUT2} = V_{DS} − 0.5 V, and SW1 = ON, the OUT1 pin current is I_{OUT1H}. Similarly, when SW2 = ON, the OUT2 pin current is I_{OUT2H}.

14. RSTO pin leakage current (I_{RSTOH}), RSTO pin sink current (I_{RSTOL})

When V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{RSTI} = V_{RSTO} =V_{CASI1} = V_{CASI2} = V_{DS}, V_{SEL1} = V_{SEL2} = 0 V, and SW4 = OFF, the RSTO pin current is I_{RSTOH}.
After setting V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{CASI1} = V_{CASI2} = V_{DS}, V_{RSTI} = V_{SEL1} = V_{SEL2} = 0 V, V_{RSTO} = 0.5 V and SW4 = ON, the self-test is performed. When the self-test is completed, the output voltage of the RSTO pin becomes "L". The RSTO pin current is defined as I_{RSTOL} at that time.

15. Detection delay time (t_{DET}), release delay time (t_{REL})

After setting V1 = V2 = V3 = V4 = V5 = V6 = V_{DU} + 0.1 V, V_{RSTI} = V_{CASI1} = V_{CASI2} = V_{DS}, V_{SEL1} = V_{SEL2} = 0 V, the voltage V4 is changed from V_{DU} + 0.1 V to V_{CU} + 1.0 V. The time interval from the V4 change until OUT1 pin output switches to the detection status is t_{DET}.
The voltage V4 is then changed from V_{CU} + 1.0 V to V_{DL} + 0.1 V. The time interval from the V4 change until OUT1 pin output switches to the release status is t_{REL}.
After changing the voltage V4 from V_{DL} + 0.1 V to V_{DL} − 1.0 V, the time until the OUT1 pin output or OUT2 pin output*1 switches to the detection status is defined as t_{DET}.
Subsequently, after changing the voltage V4 from V_{DL} − 1.0 V to V_{CU} − 0.1 V, the time until the OUT1 pin output or OUT2 pin output*1 switches to the release status is defined as t_{REL}.

***1.** When the detection signal type is "common", it is OUT1 pin output.
When the detection signal type is "separate", it is OUT2 pin output.

■ Standard Circuits

Connect the this IC according to the number of serial cells as shown below.

1. 6-serial cell (SEL1 = "High-Z", SEL2 = "High-Z")

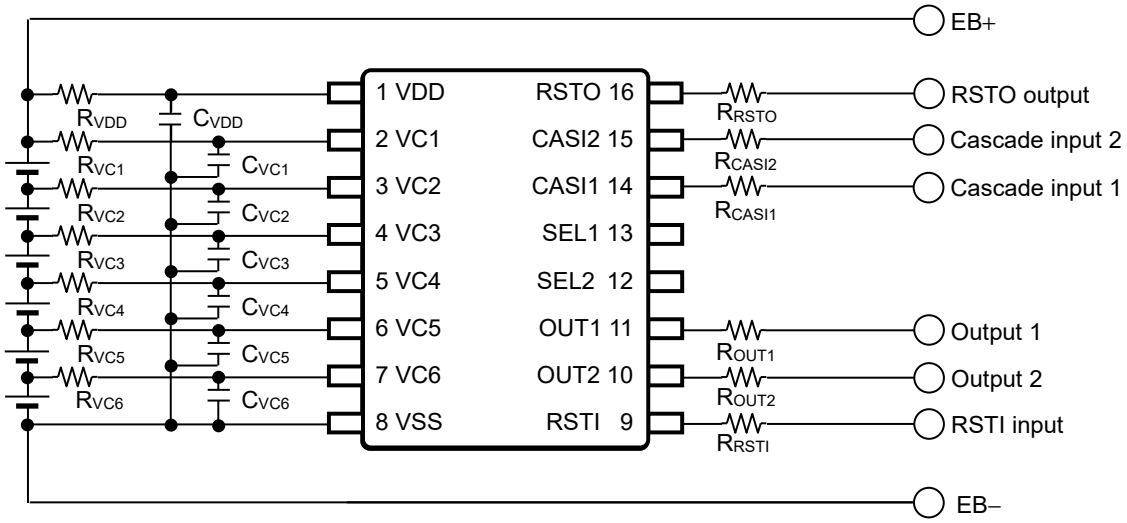


Figure 4

2. 5-serial cell (SEL1 = "High-Z", SEL2 = "H")

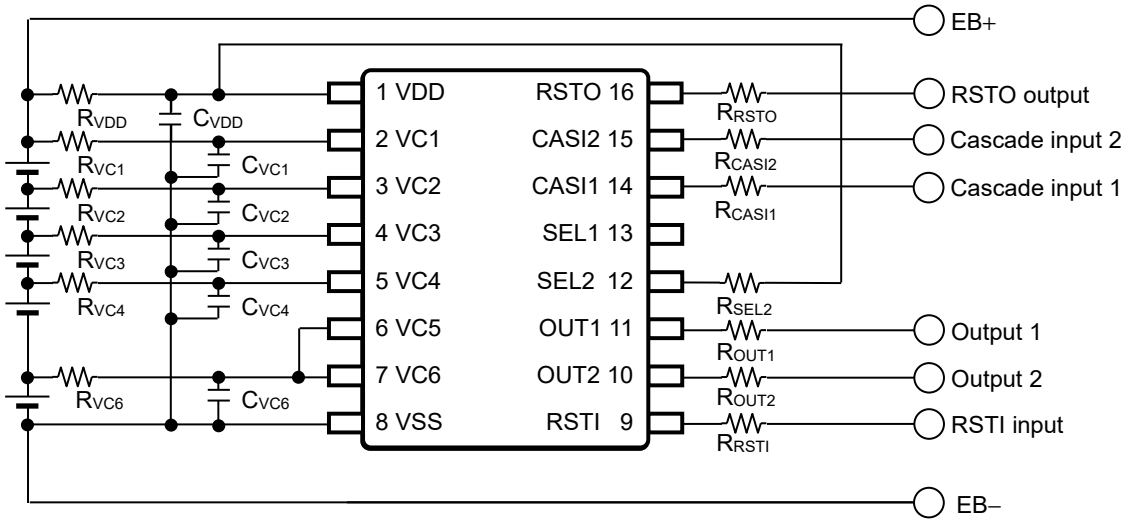


Figure 5

Remark High-Z: No connection

3. 4-serial cell (SEL1 = "H", SEL2 = "High-Z")

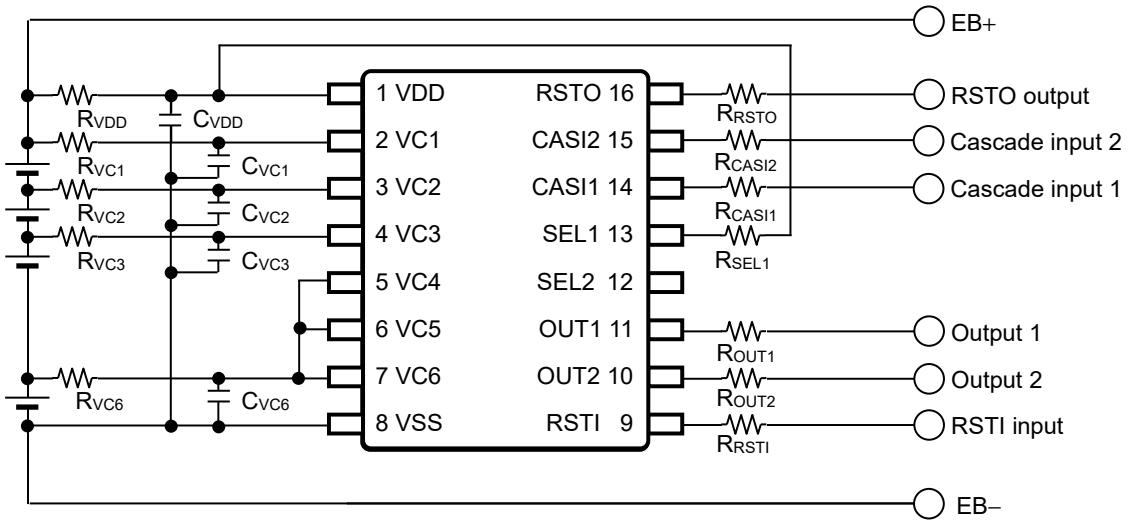


Figure 6

4. 3-serial cell (SEL1 = "H", SEL2 = "H")

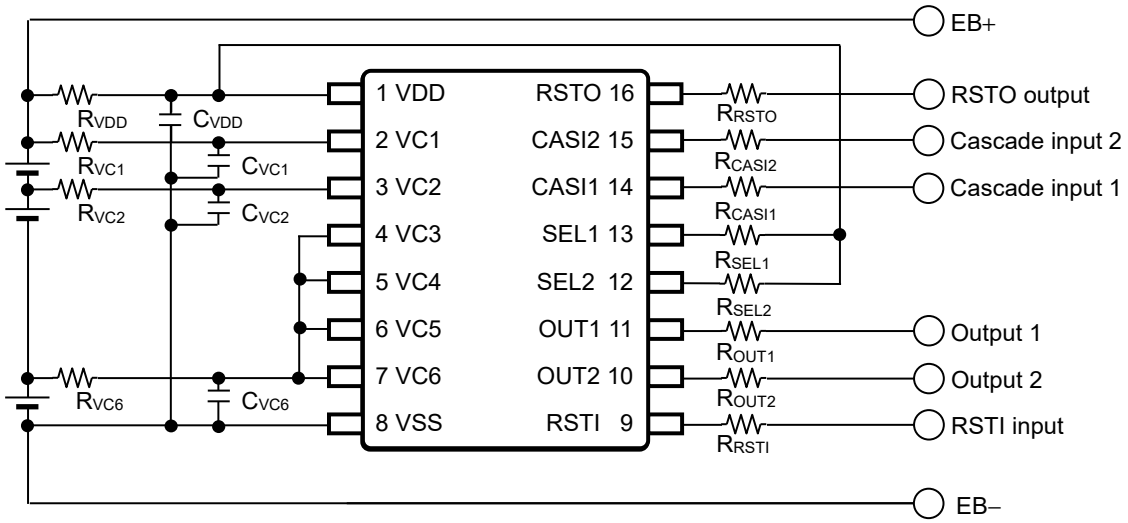


Figure 7

Remark High-Z: No connection

Table 8 Constants for External Components

Symbol	Min.	Typ.	Max.	Unit
R_{VDD}	82	100	120	Ω
R_{VCn}	0.68	1.0	1.2	kΩ
R_{SEL1}, R_{SEL2}	0.68	1.0	–	kΩ
C_{VDD}	0.68	1.0	1.5	μF
C_{VCn}	0.068	0.100	0.150	μF
R_{RSTI}	–	1.0	–	kΩ
R_{OUT1}, R_{OUT2}, R_{RSTO}	–	100	–	kΩ
R_{CASI1}, R_{CASI2}	–	1.0	–	kΩ

Caution 1. The constants may be changed without notice.
2. It has not been confirmed whether the operation is normal or not in circuits other than the connection examples. In addition, the connection examples and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.
3. Set R_{OUT1} and R_{OUT2} so that the OUT1 pin current and OUT2 pin current do not exceed 1 mA at the maximum voltage applied to this IC.
4. Set R_{RSTO} not to exceed 1 mA output current during operation.

Remark n = 1 to 6

■ Operation

1. Normal status

The voltage of all batteries is in the range from the overcharge detection voltage n (V_{CUn}) to the overdischarge detection voltage n (V_{DLn}), and additionally, the RSTI pin input voltage (V_{RSTI}) is higher than the RSTI pin voltage "H" (V_{RSTIH}), both the OUT1 and OUT2 pins output a release signal. This is the normal status.

2. Overcharge status

When the voltage of any of the batteries exceeds V_{CUn} and the status continues for the detection delay time (t_{DET}) or longer, the OUT1 pin output inverts and switches to the detection status (Refer to **Figure 9**). This is the overcharge status.
When the voltage of all batteries falls below the overcharge release voltage n (V_{CLn}) and the status continues for the release delay time (t_{REL}) or longer, the overcharge status is released and this IC returns to the normal status.

3. Overdischarge status

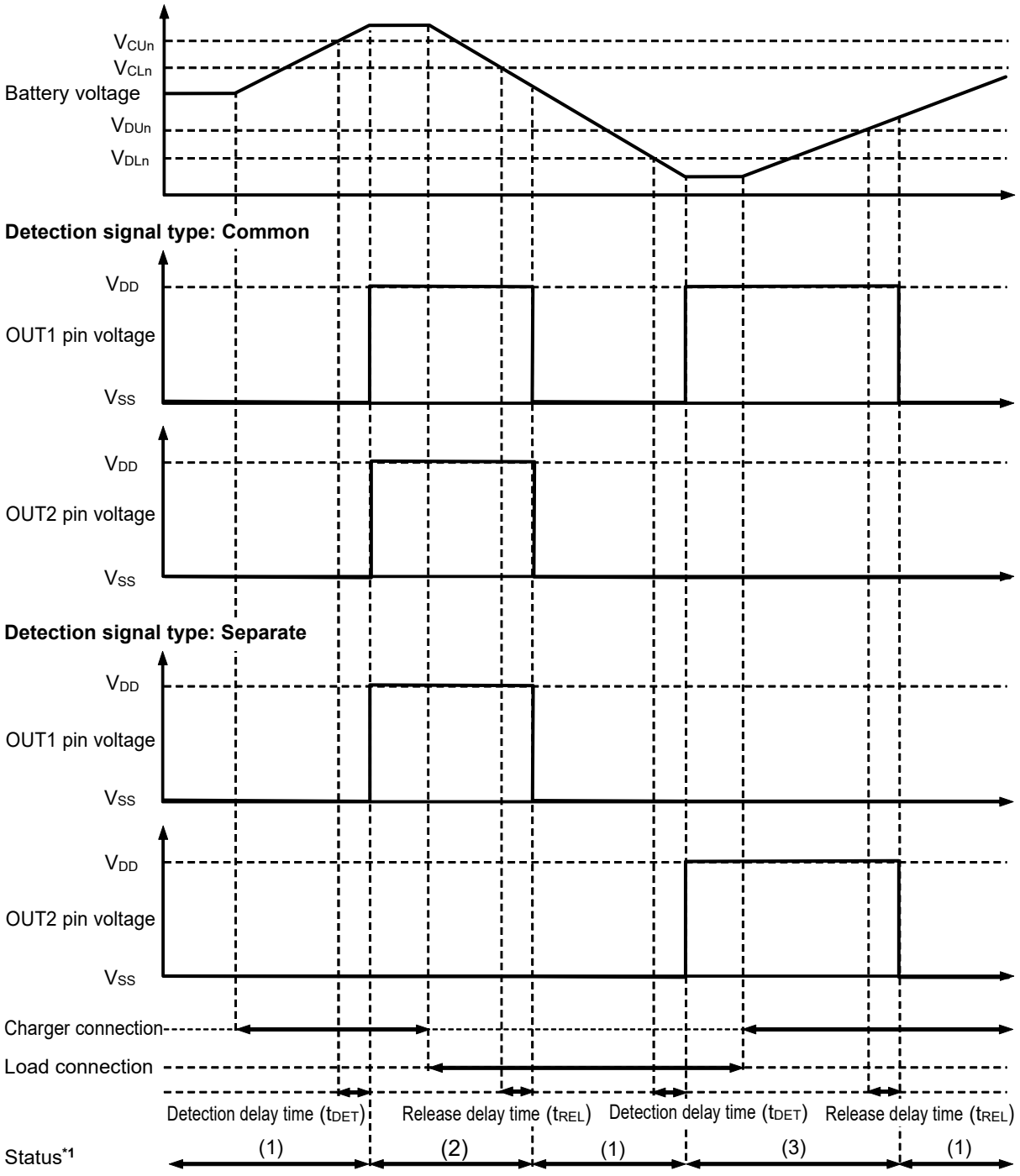
When the voltage of any of the batteries falls below V_{DLn} and the status continues for the detection delay time (t_{DET}) or longer, the OUT2 pin output[*1] inverts and switches to the detection status (Refer to **Figure 10**). This is the overdischarge status.
When the voltage of all batteries exceeds the overdischarge release voltage n (V_{DUn}) and the status continues for the release delay time (t_{REL}) or longer, the overdischarge status is released and this IC returns to the normal status.

***1.** Both outputs of OUT1 pin output and OUT2 pin output when the detection signal type is "common".

Remark **1.** Use the this IC within the range where the power supply voltage is 4.8 V or more and the voltage of each of the batteries is not lower than 0.9 V.
Also, set $V_{DLn} \times$ number of monitored cells $>$ 4.8 V
2. n = 1 to 6

■ Timing Charts

1. Overcharge detection and overdischarge detection

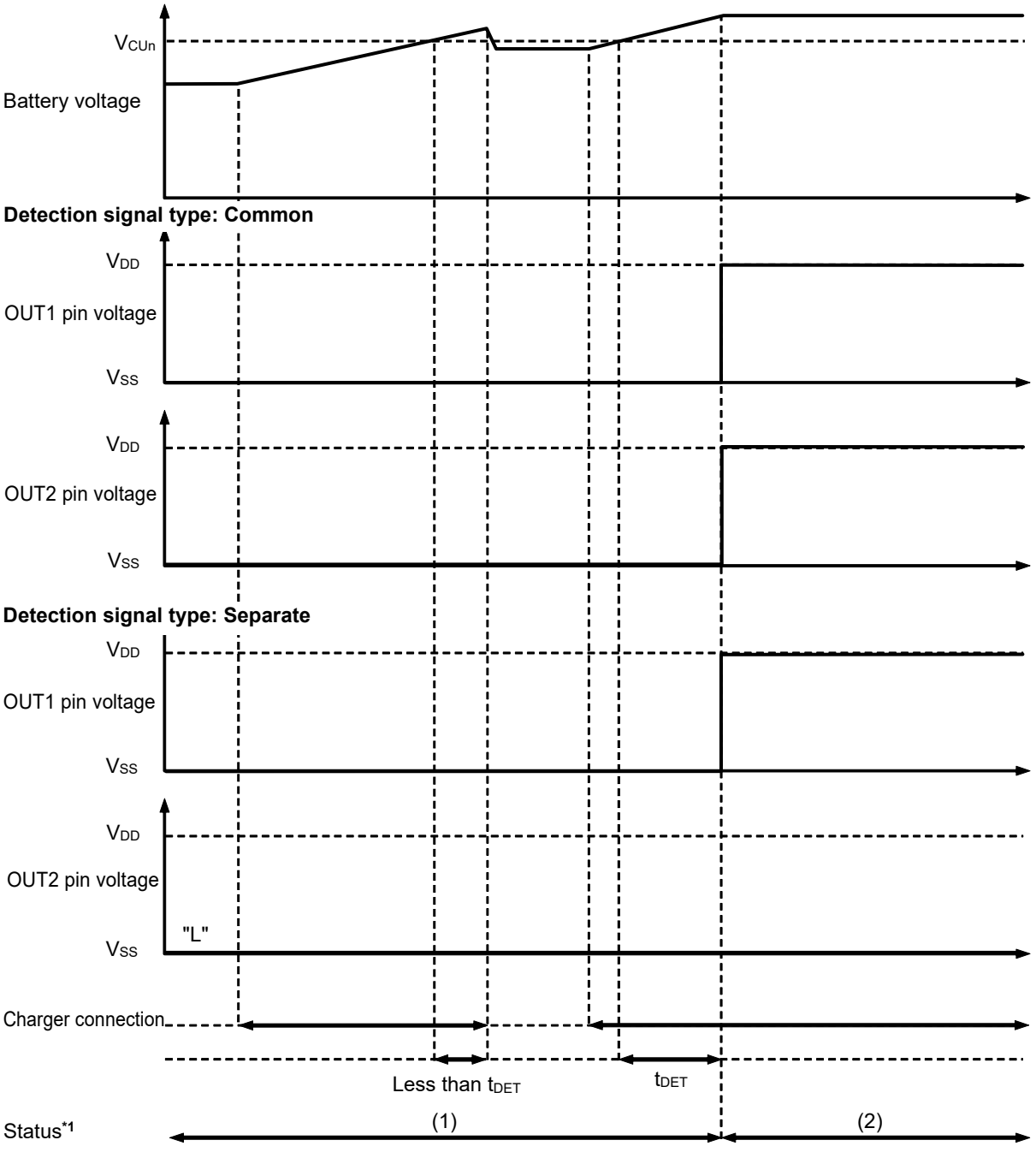


***1.** (1): Normal status
(2): Overcharge status
(3): Overdischarge status

Figure 8

Remark n = 1 to 6

2. Overcharge detection delay

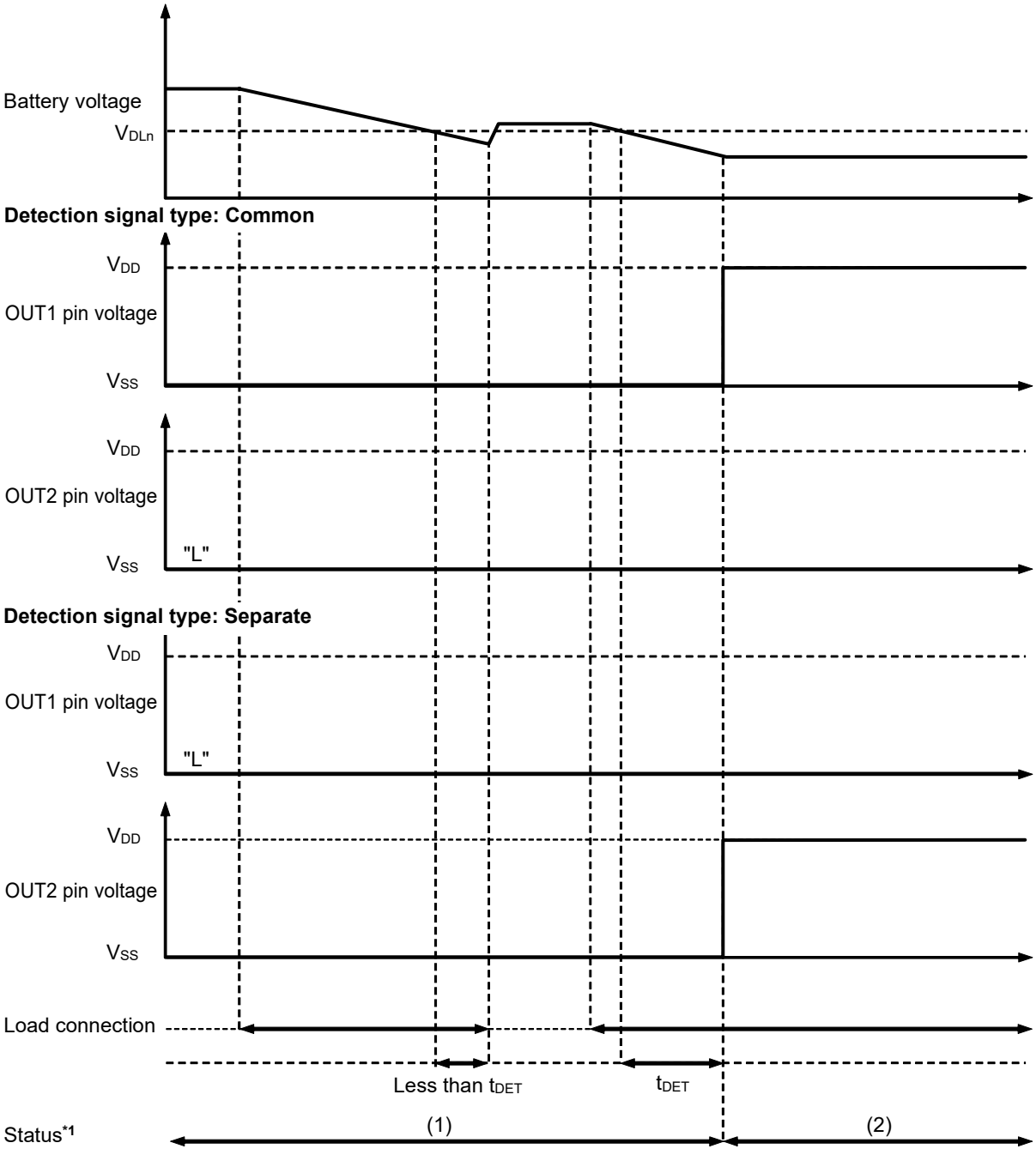


***1.** (1): Normal status
(2): Overcharge status

Figure 9

Remark n = 1 to 6

3. Overdischarge detection delay



***1.** (1): Normal status
(2): Overdischarge status

Figure 10

Remark n = 1 to 6

■ Self-test Function

This IC has a self-test function to confirm overcharge and overdischarge detection operations.
Due to the self-test function, a current flows in internal voltage-dividing resistors, comparator input voltage changes, and then this IC spuriously switches to the overcharge or overdischarge status. It is possible to confirm whether this IC normally detects the overcharge and overdischarge or not by monitoring the OUT1 pin and OUT2 pin output signals.

Remark The self-test is not normally performed under the following conditions.

- When this IC is in the overcharge or overdischarge status
- When the power supply voltage is 4.8 V or lower

1. Self-test input signal

1. 1 RSTI (reset signal) input

When "L" is input to the RSTI pin, the self-test starts. When "H" is input, this IC returns to the normal operation.

1. 2 Self-test input signal timing charts

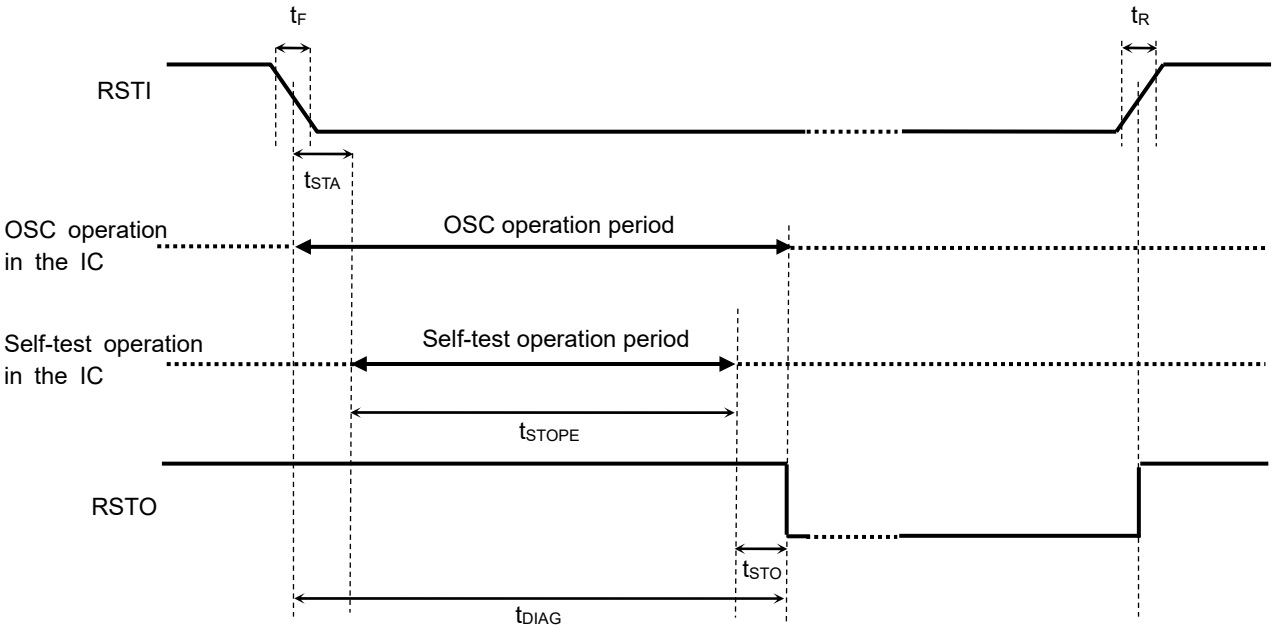


Figure 11

Remark t_R, t_F = 300 ns max.
t_{STA} = 10 ms typ.
t_{STOPE} = 54 ms typ.
t_{STO} = 2 ms typ.
t_{DIAG} = 66 ms typ.

t_R: RSTI rising time
t_F: RSTI falling time
t_{STA}: Self-test start time (Time period from reset signal falling to start of self-test output)
t_{STOPE}: Self-test running time (Time period from start to end of self-test operation)
t_{STO}: Self-test end time (Time period from falling edge at end of LVREG diagnosis to start of RSTO output) (Even if RSTI becomes "H" during the self-test operation time, the diagnosis will be performed to the end. Refer to **Figure 21**.)
t_{DIAG}: Diagnosis time (Time required for diagnosis per 1 IC)

2. Operation of self-test function

2. 1 Self-test for overcharge detection (n = 1 to 2)

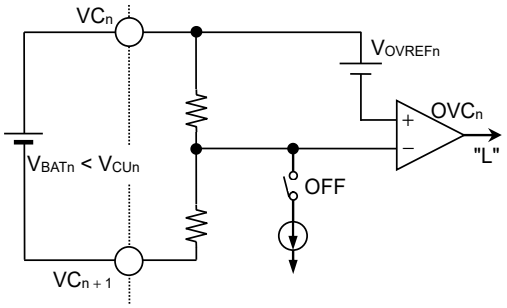


Figure 12 Non-detection operation during self-test operation

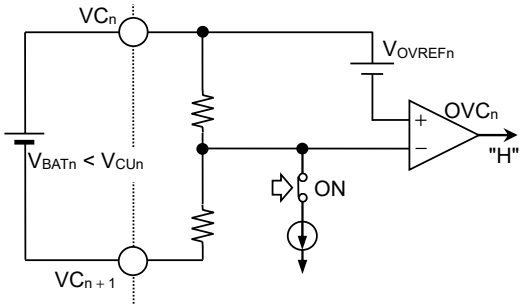
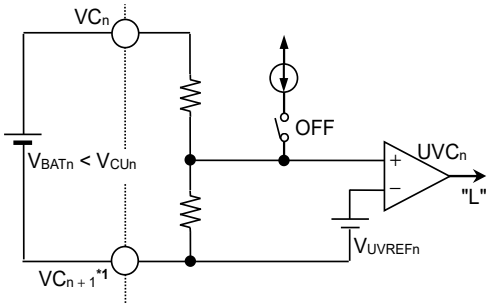


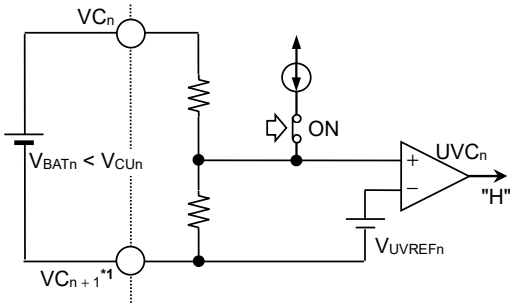
Figure 13 Detection operation during self-test operation

2. 2 Self-test for overcharge detection (n = 3 to 6)



***1.** When n = 6, it is VSS pin.

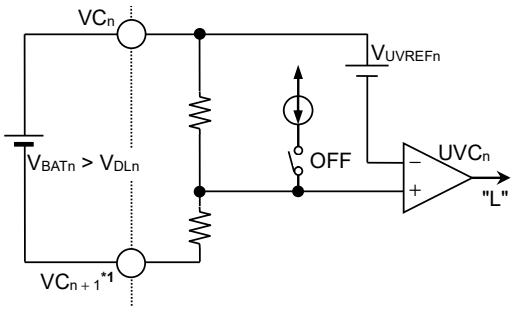
Figure 14 Non-detection operation during self-test operation



***1.** When n = 6, it is VSS pin.

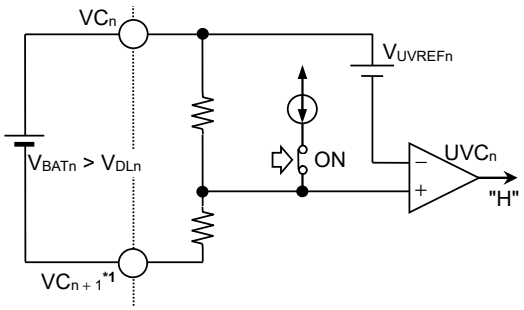
Figure 15 Detection operation during self-test operation

2. 3 Self-test for overdischarge detection (n = 1 to 5)



***1.** When n = 6, it is VSS pin.

Figure 16 Non-detection operation during self-test operation



***1.** When n = 6, it is VSS pin.

Figure 17 Detection operation during self-test operation

2. 4 Self-test for overdischarge detection (Battery 6)

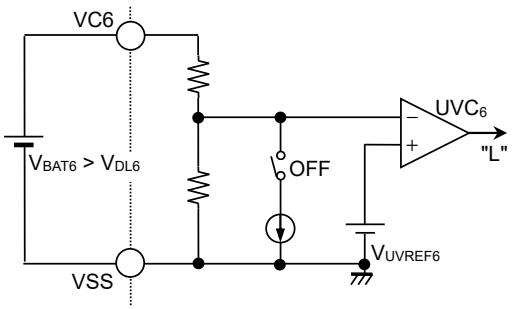


Figure 18 Non-detection operation during self-test operation

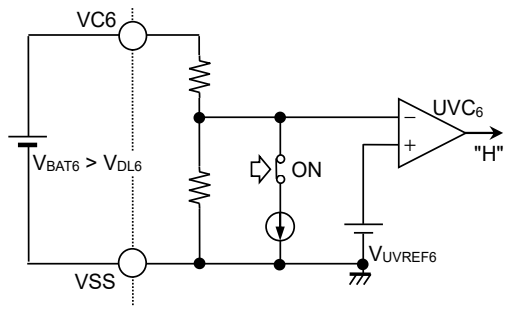


Figure 19 Detection operation during self-test operation

3. Self-test output signal

3. 1 No failure

3. 1. 1 Overcharge detection diagnosis

When "L" is input to the RSTI pin for a certain period of time, the self-test is performed starting from the upper cell. The overcharge detection signal is output to OUT1 pin and OUT2 pin whether the detection signal type is common or separate (Refer to **Figure 20** and **Figure 25**).

3. 1. 2 Overdischarge detection diagnosis

When "L" is input to the RSTI pin for a certain period of time, the self-test is performed in order from the upper cell. The overdischarge detection signal is output from the OUT1 pin when the detection signal type is common, and from the OUT2 pin when it is separate (Refer to **Figure 20** and **Figure 25**).

3. 1. 3 LV regulator diagnosis

When "L" is input to the RSTI pin for a certain period of time, the self-test is performed starting from the upper cell. After the UV6 diagnosis pulse output, diagnosis of high-voltage and low-voltage abnormalities in the LV regulator is performed. Regardless of whether the detection signal type is common or separate, the OUT1 and OUT2 pins output "H" at the 14th clocks (LVREG) from the self-test start (Refer to **Figure 20** and **Figure 25**).

3. 2 In case of failure

3. 2. 1 In case of overcharge detection function and overdischarge detection function failure

The output of the fault location does not switch to the detection status.

3. 2. 2 In case of LV regulator failure

Either the OUT1 pin output or OUT2 pin output "H" immediately after the self-test starts and returns to "L" after the self-test operation time is over (Refer to **Figure 23, Figure 24, Figure 30,** and **Figure 31**).

Remark n = 1 to 6

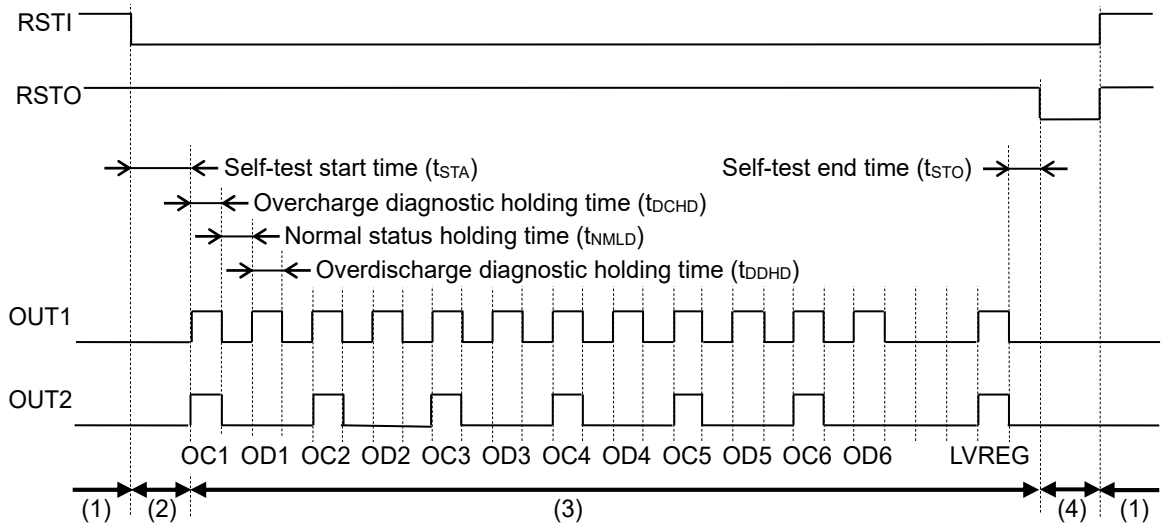
Table 9 OUT1 Pin and OUT2 Pin Outputs during Self-test

Output Combination	Mode	OUT1 Pin	OUT2 Pin
Detection signal type: Common	Normal	Overcharge detection result Overdischarge detection result	Overcharge detection result
	Self-test	Overcharge detection diagnosis Overdischarge detection diagnosis LV regulator diagnosis	Overcharge detection diagnosis LV regulator diagnosis
Detection signal type: Separate	Normal	Overcharge detection result	Overdischarge detection result
	Self-test	Overcharge detection diagnosis LV regulator diagnosis	Overcharge detection diagnosis Overdischarge detection diagnosis LV regulator diagnosis

4. Operation Example of Self-test Function

4. 1 6-serial cell, detection signal type: Common

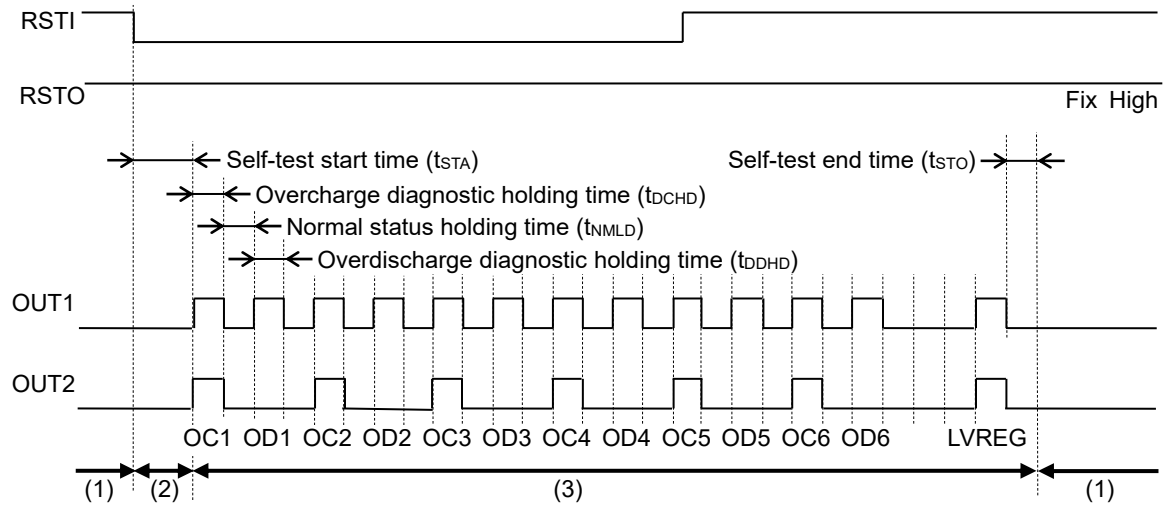
4. 1. 1 No failure



(1): Normal status
(2): Self-test setup time
(3): Self-test execution status
(4): Self-test upper input standby status

Figure 20

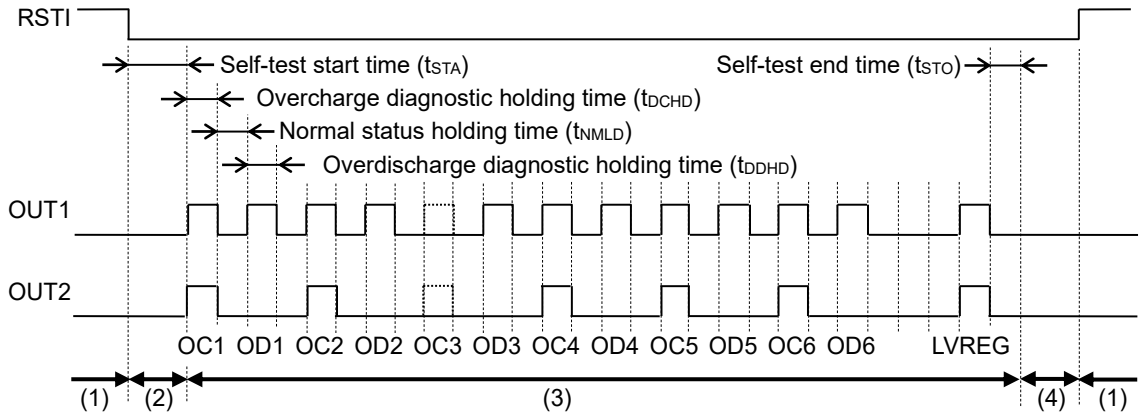
4. 1. 2 No failure: Self-test interruption



(1): Normal status
(2): Self-test setup time
(3): Self-test execution status

Figure 21

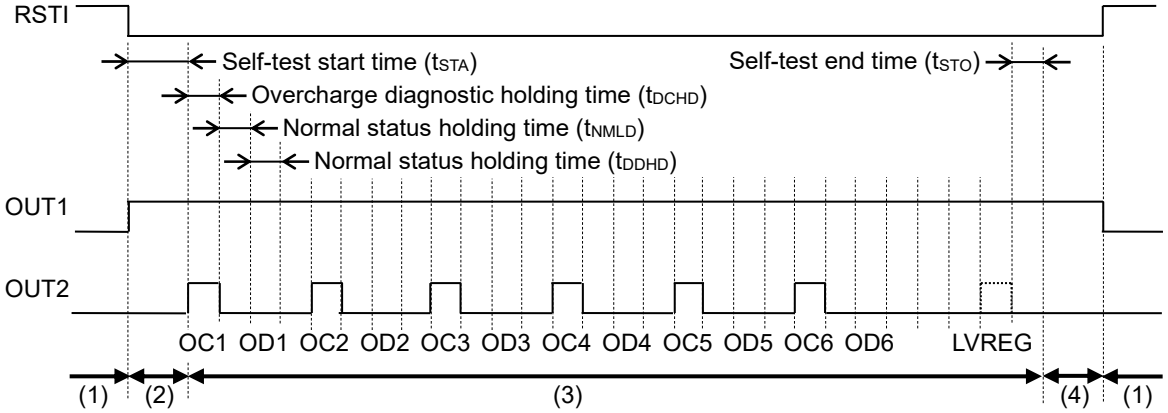
4. 1. 3 In case of failure: Overcharge detection fault (OC3)



(1): Normal status
(2): Self-test setup time
(3): Self-test execution status
(4): Self-test upper input standby status

Figure 22

4. 1. 4 In case of failure: LV regulator high voltage fault

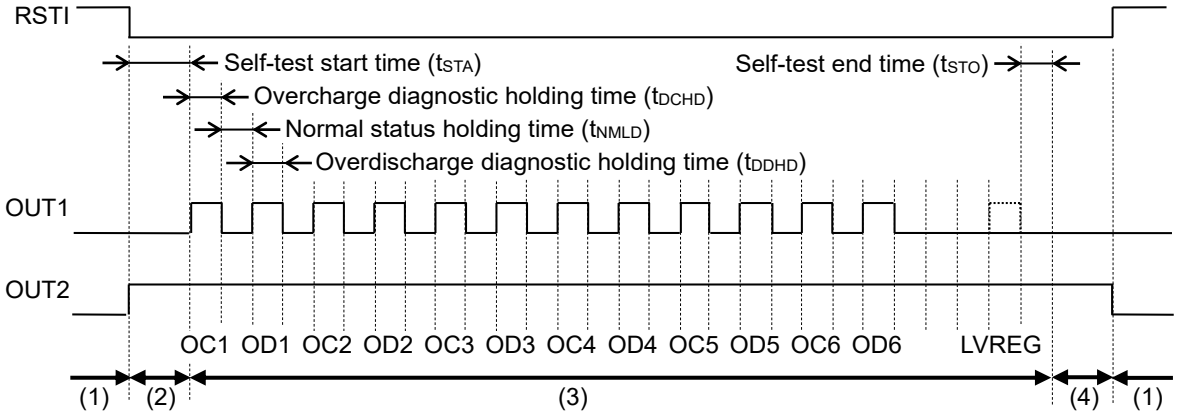


(1): Normal status
(2): Self-test setup time
(3): Self-test execution status
(4): Self-test upper input standby status

Figure 23

Caution In case of circuit breakage due to high voltage, OUT2 pin output may not have the above waveform.

4. 1. 5 In case of failure: LV regulator low voltage fault



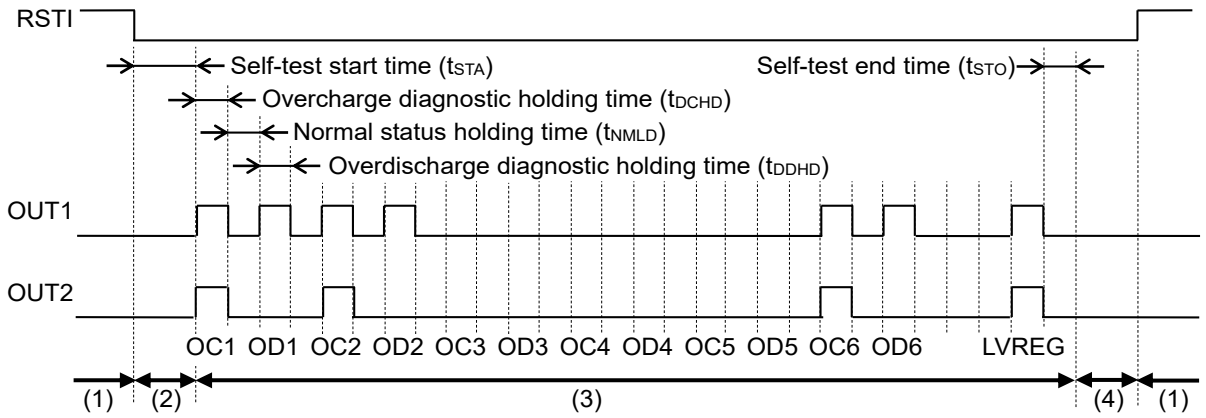
(1): Normal status
(2): Self-test setup time
(3): Self-test execution status
(4): Self-test upper input standby status

Figure 24

Caution If the circuit cannot operate due to low voltage, OUT1 pin output may not have the above waveform.

4. 2 3-serial cell, detection signal type: Common

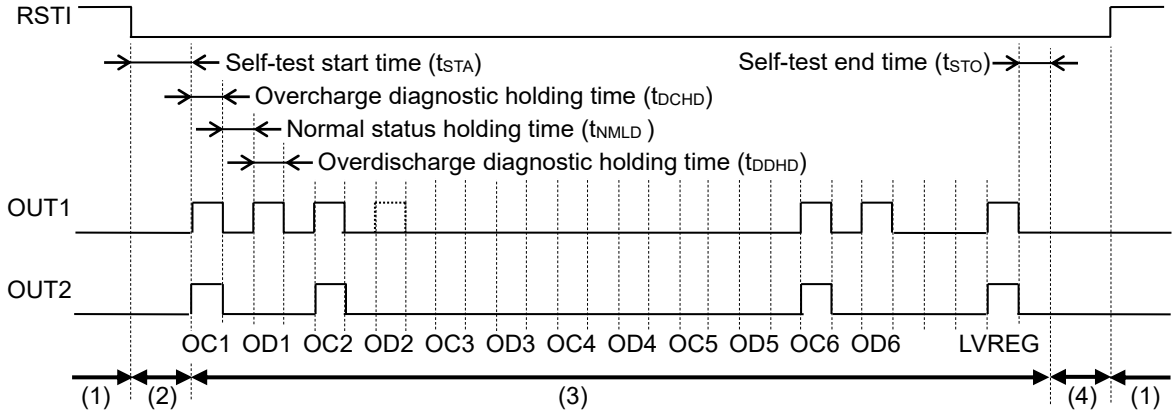
4. 2. 1 No failure



(1): Normal status
(2): Self-test setup time
(3): Self-test execution status
(4): Self-test upper input standby status

Figure 25

4. 2. 2 In case of failure: Overdischarge detection fault (OD2)

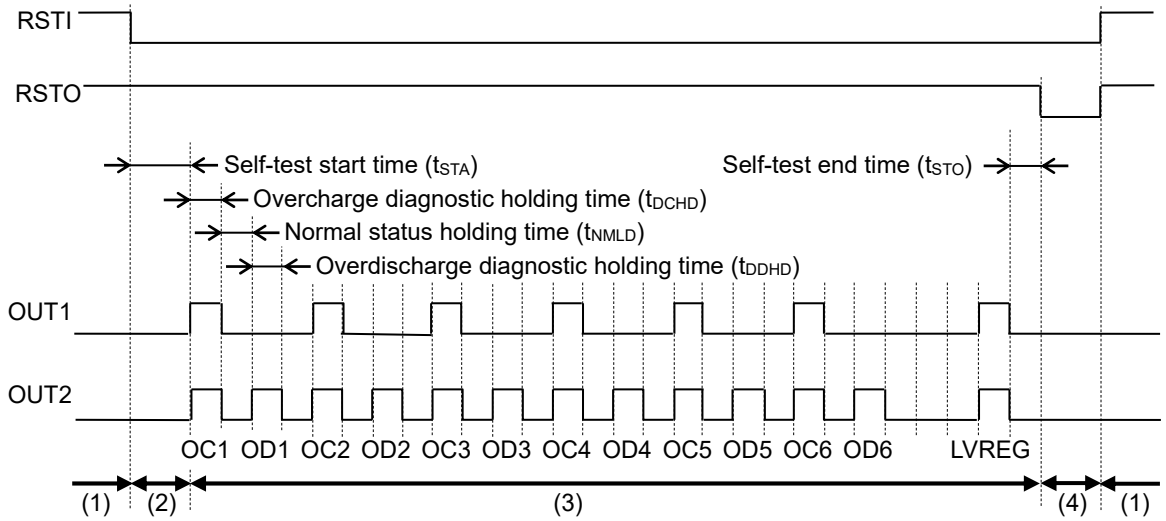


(1): Normal status
(2): Self-test setup time
(3): Self-test execution status
(4): Self-test upper input standby status

Figure 26

4. 3 6-serial cell, detection signal type: Separate

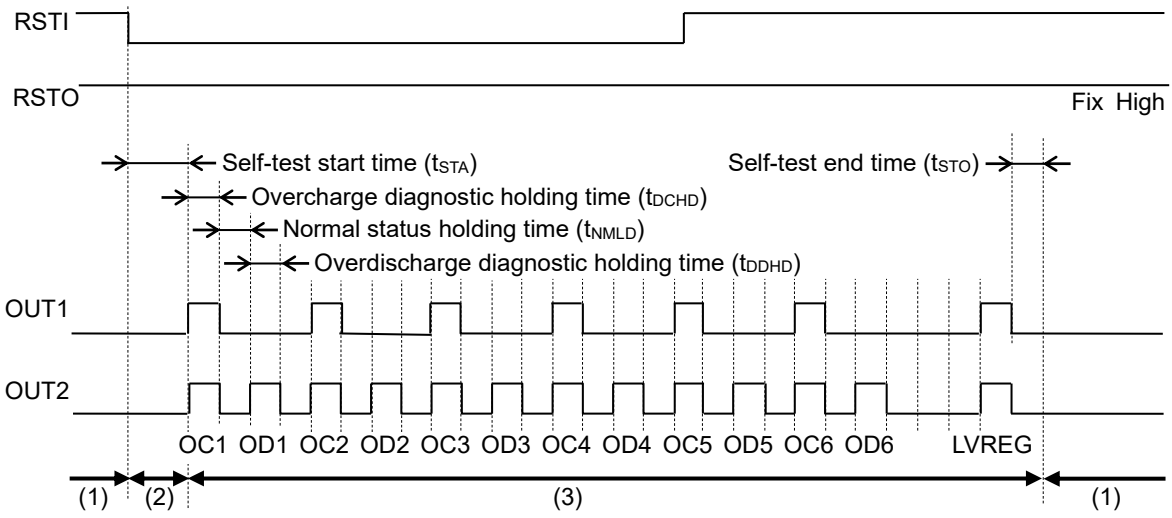
4. 3. 1 No failure



(1): Normal status
(2): Self-test setup time
(3): Self-test execution status
(4): Self-test upper input standby status

Figure 27

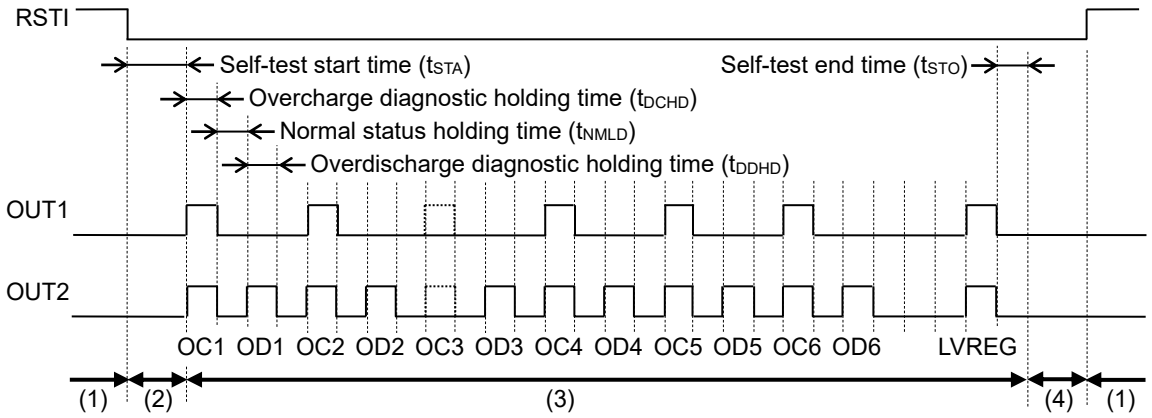
4. 3. 2 No failure: Self-test interruption



(1): Normal status
(2): Self-test setup time
(3): Self-test execution status

Figure 28

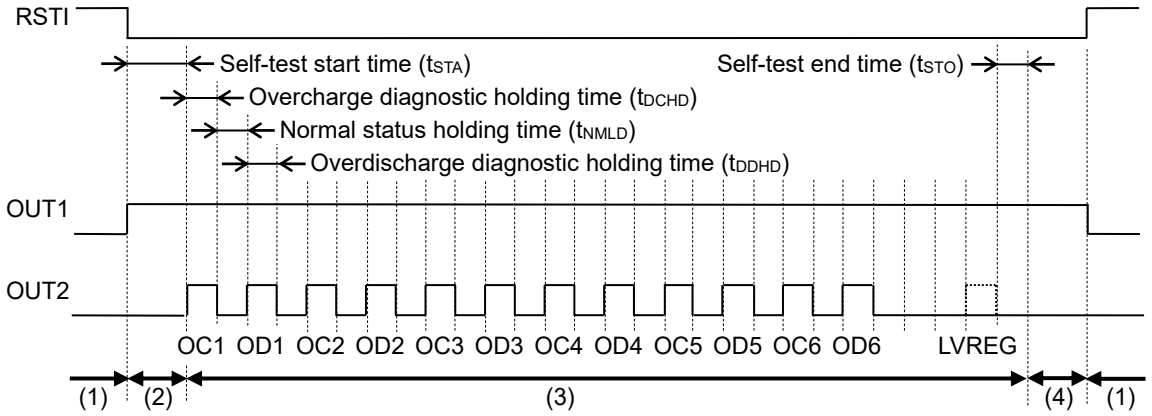
4. 3. 3 In case of failure: Overcharge detection fault (OC3)



(1): Normal status
(2): Self-test setup time
(3): Self-test execution status
(4): Self-test upper input standby status

Figure 29

4. 3. 4 In case of failure: LV regulator high voltage fault

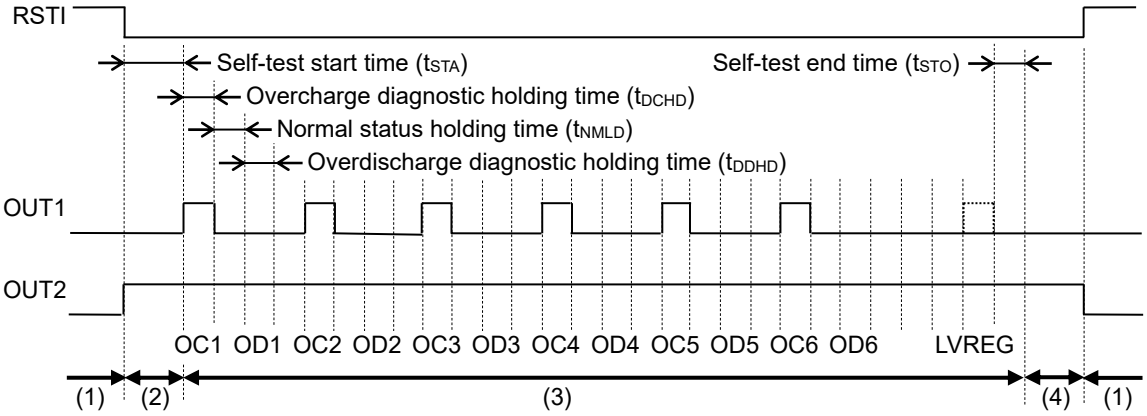


(1): Normal status
(2): Self-test setup time
(3): Self-test execution status
(4): Self-test upper input standby status

Figure 30

Caution In case of circuit breakage due to high voltage, OUT2 pin output may not have the above waveform.

4. 3. 5 In case of failure: LV regulator low voltage fault



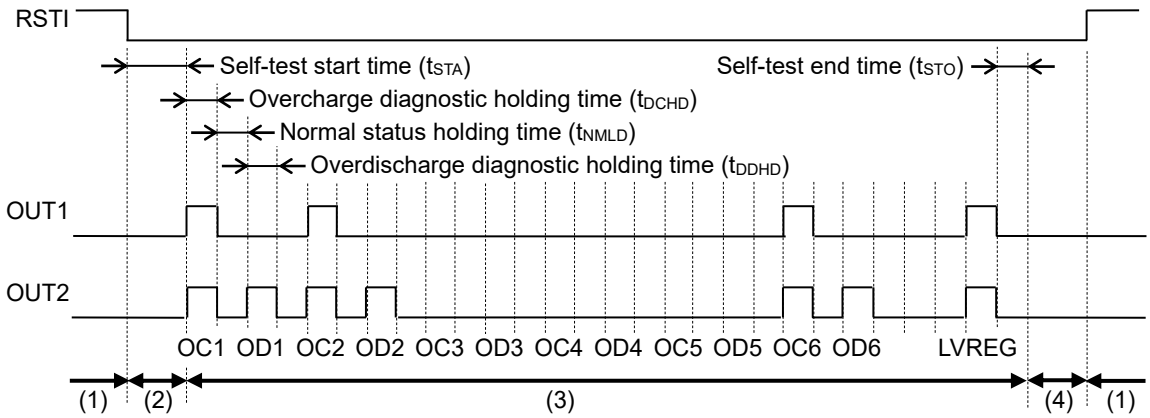
(1): Normal status
(2): Self-test setup time
(3): Self-test execution status
(4): Self-test upper input standby status

Figure 31

Caution If the circuit cannot operate due to low voltage, OUT1 pin output may not have the above waveform.

4. 4 3-serial cell, detection signal type: Separate

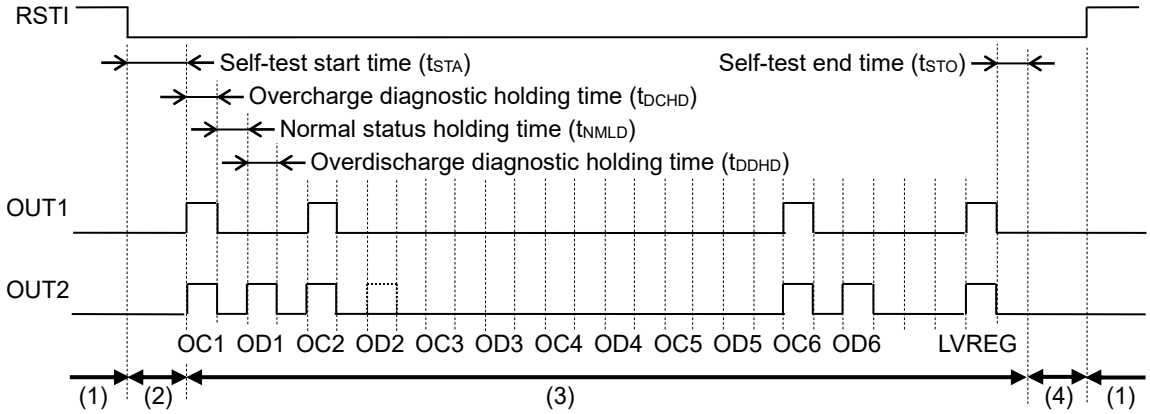
4. 4. 1 No failure



(1): Normal status
(2): Self-test setup time
(3): Self-test execution status
(4): Self-test upper input standby status

Figure 32

4. 4. 2 In case of failure: Overdischarge detection fault (OD2)



(1): Normal status
(2): Self-test setup time
(3): Self-test execution status
(4): Self-test upper input standby status

Figure 33

■ Battery Protection IC Connection Example For Multi-serial-cell Pack

1. 9-serial cell (5-serial cell + 4-serial cell, cascade DC connection)

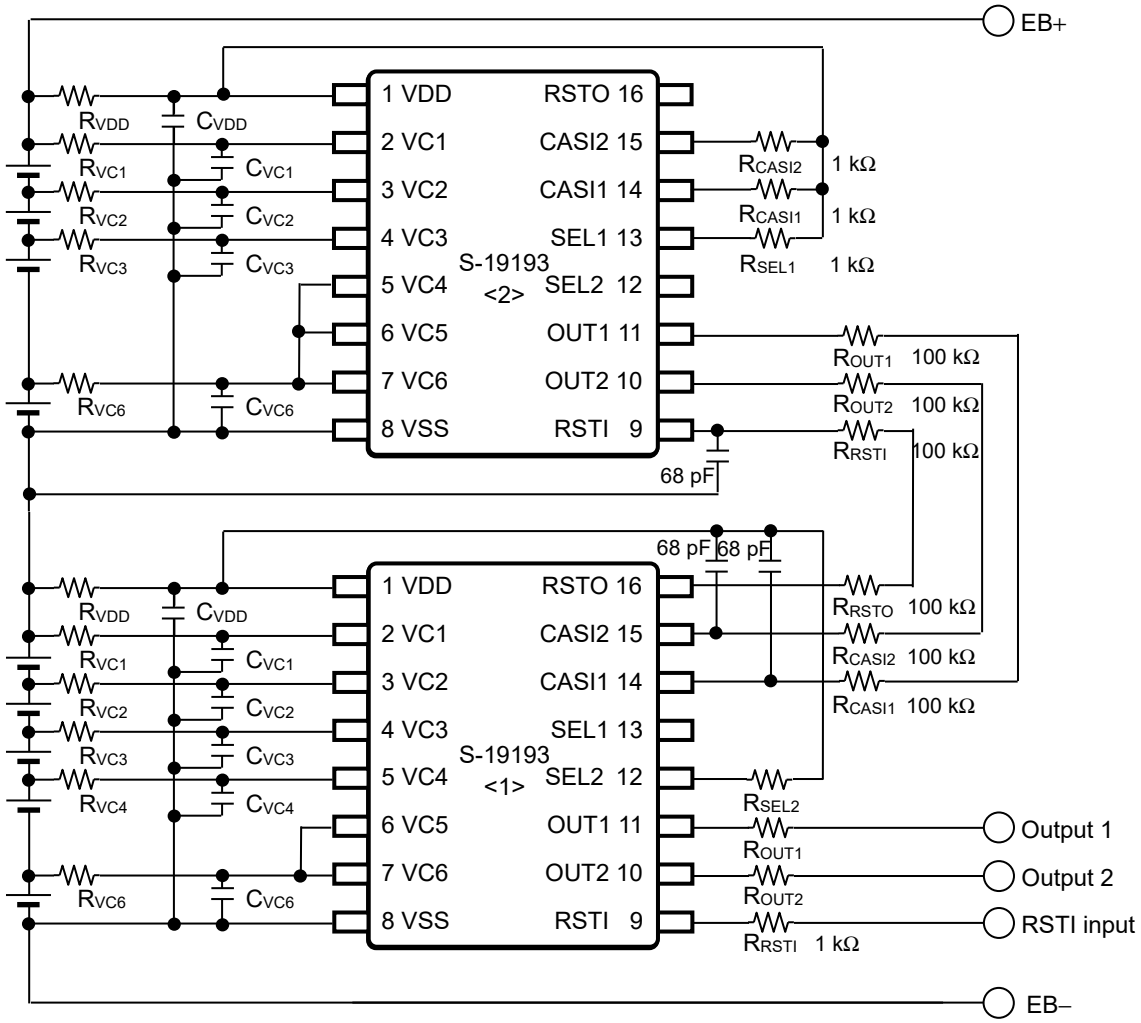


Figure 34

Remark For communication resistors (R_{OUT1}, R_{OUT2}, R_{RSTI}, R_{RSTO}, R_{CASI1}, R_{CASI2}) at the time of cascade DC connection, a resistor of 100 kΩ or more is recommended.

Table 10 Constants for External Components

Symbol	Min.	Typ.	Max.	Unit
R_{VDD}	82	100	120	Ω
R_{VCn}	0.68	1.0	1.2	kΩ
R_{SEL1}, R_{SEL2}	0.68	1.0	–	kΩ
C_{VDD}	0.68	1.0	1.5	μF
C_{VCn}	0.068	0.100	0.150	μF
R_{RSTI}	-	1.0	-	kΩ
R_{RSTI} (DC)*1	-	100	-	kΩ
R_{OUT1}, R_{OUT2}, R_{RSTO}	-	100	-	kΩ
R_{CASI1}, R_{CASI2}	-	1.0	-	kΩ
R_{CASI1}, R_{CASI2} (DC)*2	-	100	-	kΩ

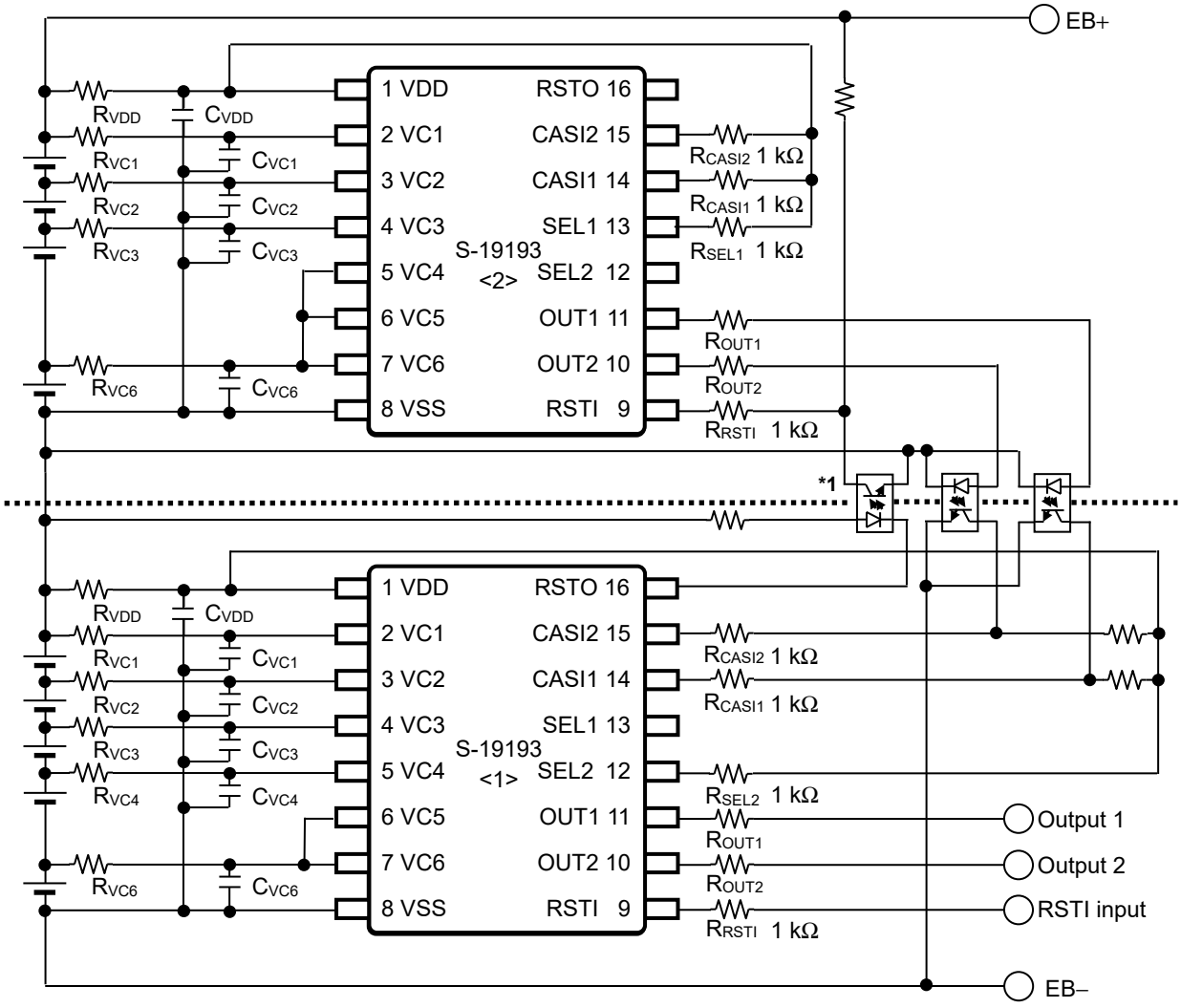
***1.** R_{RSTI} (DC): Recommended value for this IC in the upper module during cascade DC connection communication (Refer to **Figure 34**).

***2.** R_{CASI1}, R_{CASI2} (DC): Recommended values for this IC in the lower module during cascade DC connection communication (Refer to **Figure 34**).

Caution 1. The constants may be changed without notice.
2. It has not been confirmed whether the operation is normal or not in circuits other than the connection examples. In addition, the connection examples and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.
3. Set R_{OUT1} and R_{OUT2} so that the OUT1 pin current and OUT2 pin current do not exceed 1 mA at the maximum voltage applied to this IC.
4. Set R_{RSTO} not to exceed 1 mA output current during operation.

Remark n = 1 to 6

2. 9-serial cell (5-serial cell + 4-serial cell, isolated cascade connection)



***1.** Isolation between modules by photocoupler

Figure 35

Remark 1. For communication input resistors (R_{RSTI}, R_{CASI1}, R_{CASI2}) at the time of isolated cascade connection, a resistor of 1 kΩ is recommended.

2. Resistors not listed with numbers and symbols should be selected according to the actual battery voltage.

Table 11 Constants for External Components

Symbol	Min.	Typ.	Max.	Unit
R_{VDD}	82	100	120	Ω
R_{VCn}	0.68	1.0	1.2	kΩ
R_{SEL1}, R_{SEL2}	0.68	1.0	–	kΩ
C_{VDD}	0.68	1.0	1.5	μF
C_{VCn}	0.068	0.100	0.150	μF
R_{RSTI}	-	1.0	-	kΩ
R_{OUT1}, R_{OUT2}, R_{RSTO}	-	100	-	kΩ
R_{CASI1}, R_{CASI2}	-	1.0	-	kΩ

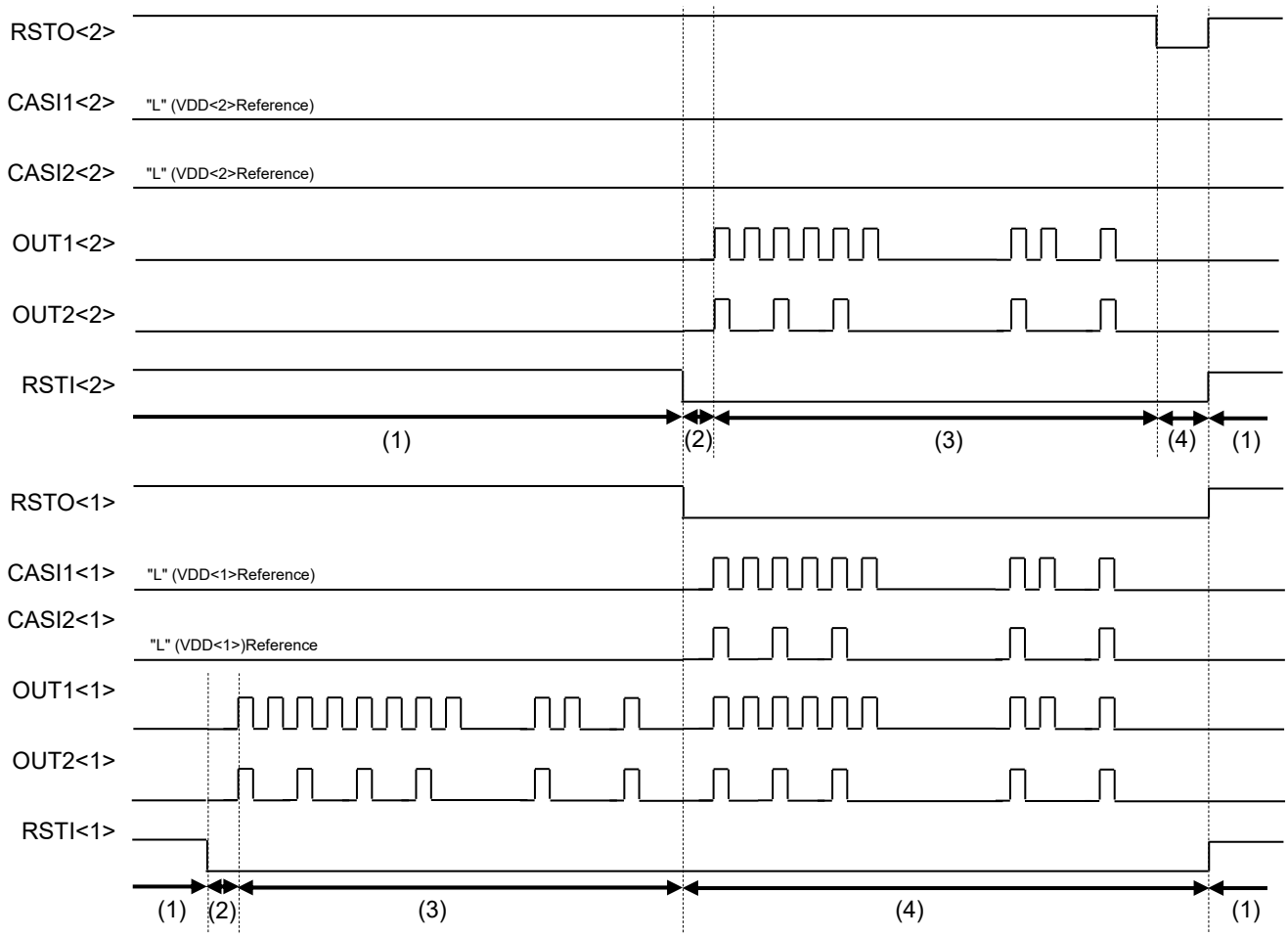
Caution 1. The constants may be changed without notice.
2. It has not been confirmed whether the operation is normal or not in circuits other than the connection examples. In addition, the connection examples and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.
3. Set R_{OUT1} and R_{OUT2} so that the OUT1 pin current and OUT2 pin current do not exceed 1 mA at the maximum voltage applied to this IC.
4. Set R_{RSTO} not to exceed 1 mA output current during operation.

Remark n = 1 to 6

3. Timing chart at Cascade connection

3. 1 5-serial cell + 4-serial cell, detection signal type: Common

3. 1. 1 No failure



(1): Normal status
(2): Self-test setup time
(3): Self-test execution status
(4): Self-test upper input standby status

Figure 36

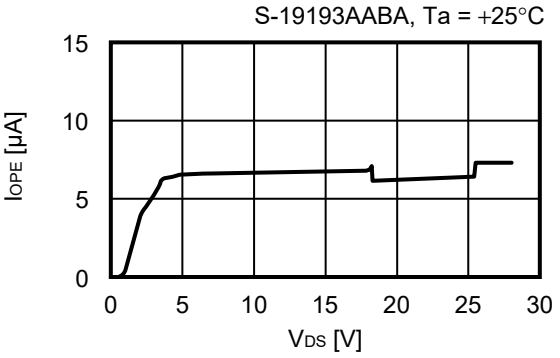
■ Precautions

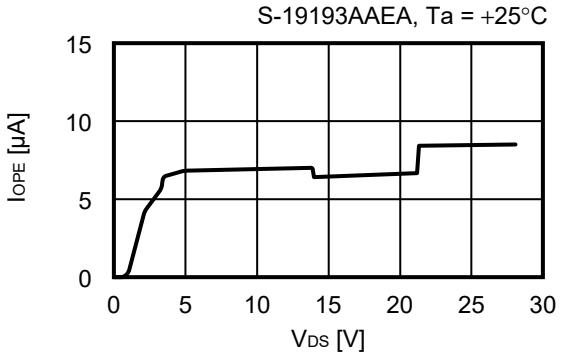
- The application conditions for the input voltage, output voltage, and load current should not exceed the power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Characteristics (Typical Data)

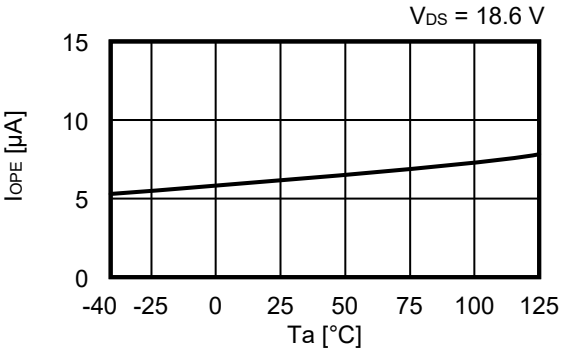
1. Current consumption

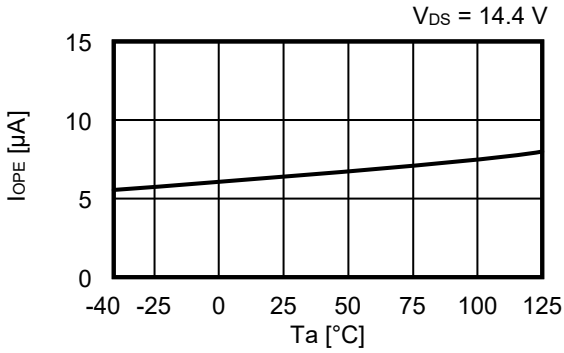
1. 1 I_{OPE} vs. V_{DS}



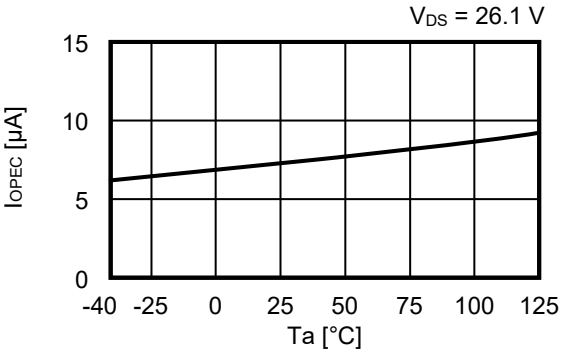


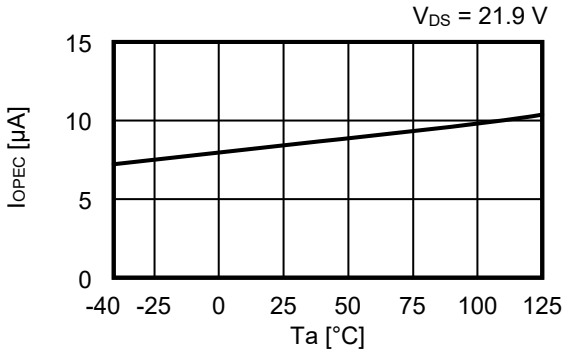
1. 2 I_{OPE} vs. Ta



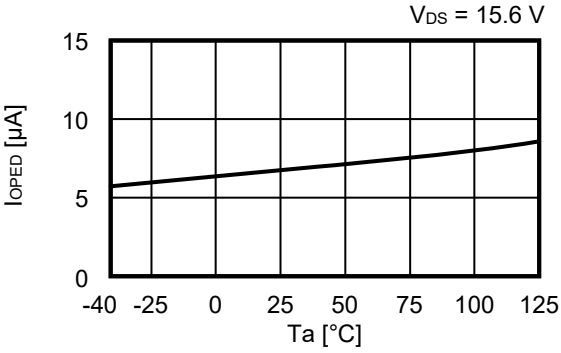


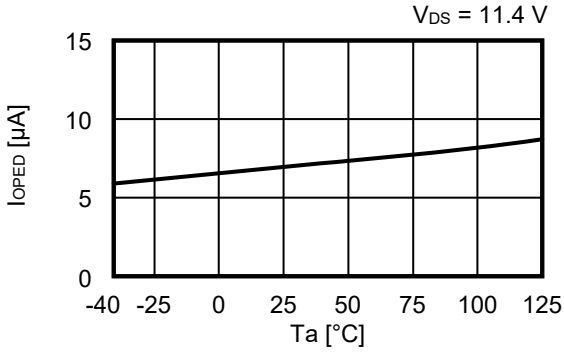
1. 3 I_{OPEC} vs. Ta





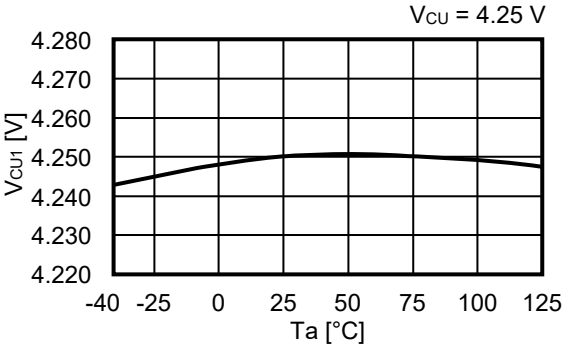
1. 4 I_{OPED} vs. Ta



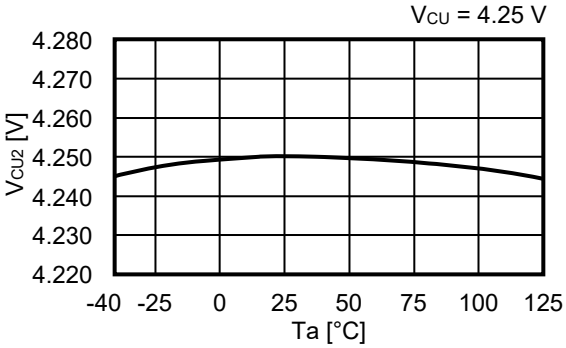


2. Detection voltage, release voltage

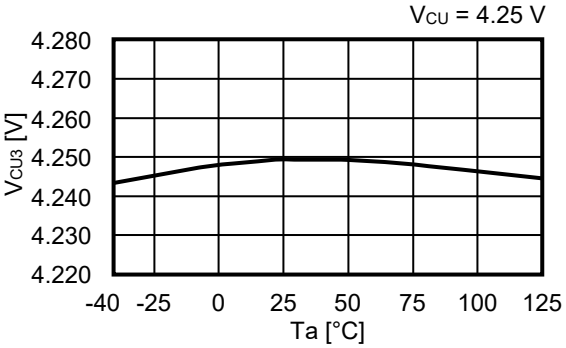
2. 1 V_{CU1} vs. Ta



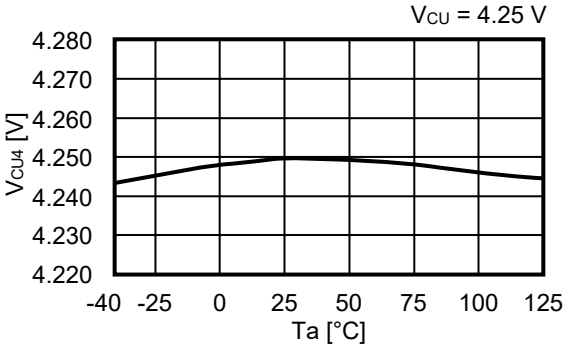
2. 2 V_{CU2} vs. Ta



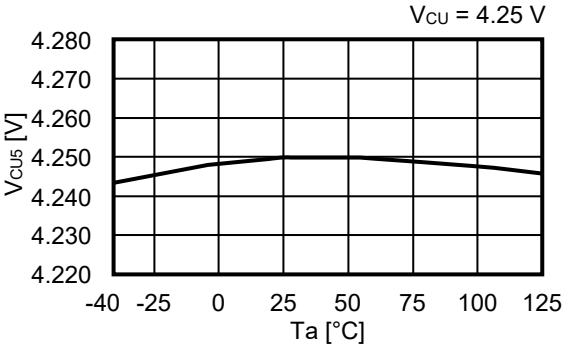
2. 3 V_{CU3} vs. Ta



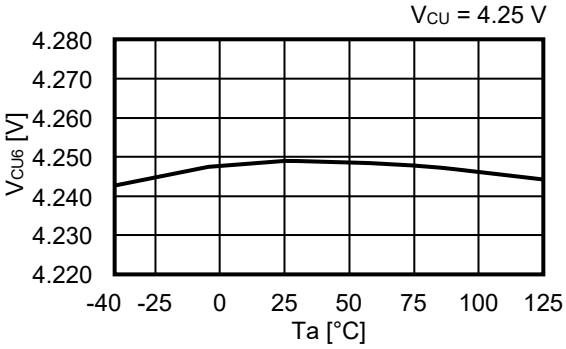
2. 4 V_{CU4} vs. Ta



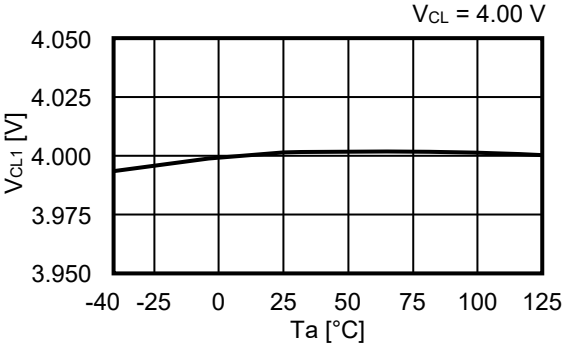
2. 5 V_{CU5} vs. Ta



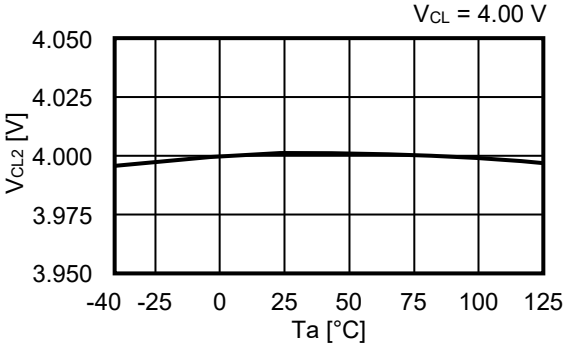
2. 6 V_{CU6} vs. Ta



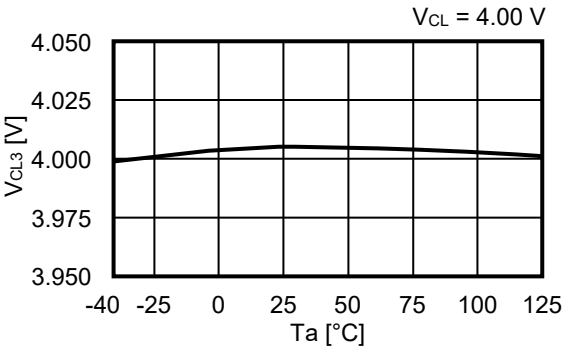
2. 7 V_{CL1} vs. Ta



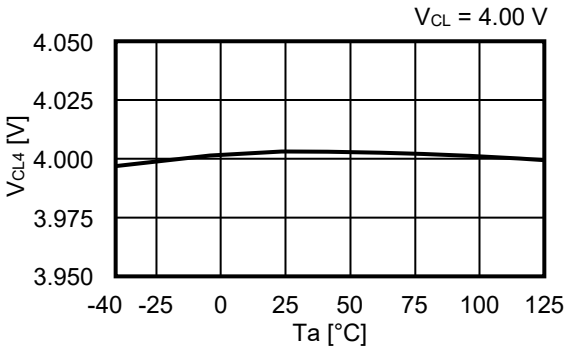
2. 8 V_{CL2} vs. Ta



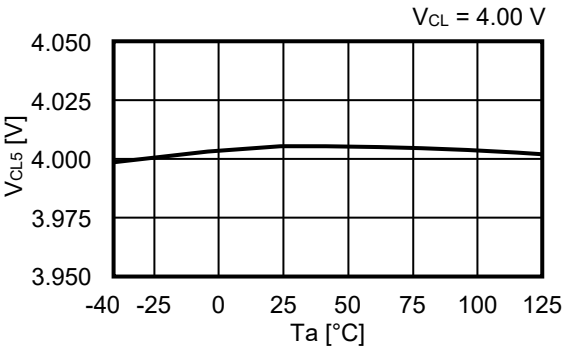
2. 9 V_{CL3} vs. Ta



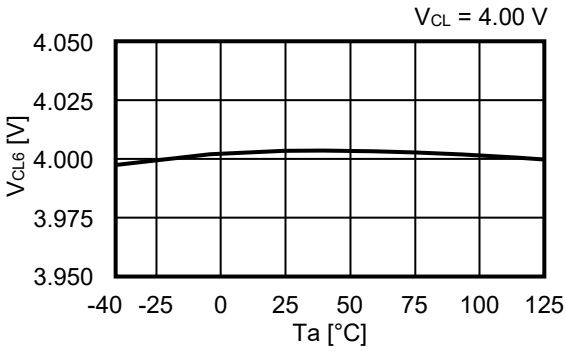
2. 10 V_{CL4} vs. Ta



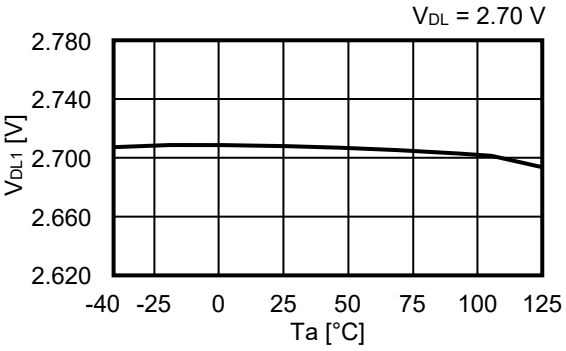
2. 11 V_{CL5} vs. Ta



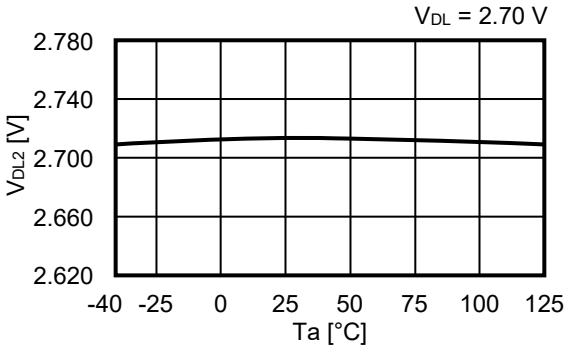
2. 12 V_{CL6} vs. Ta



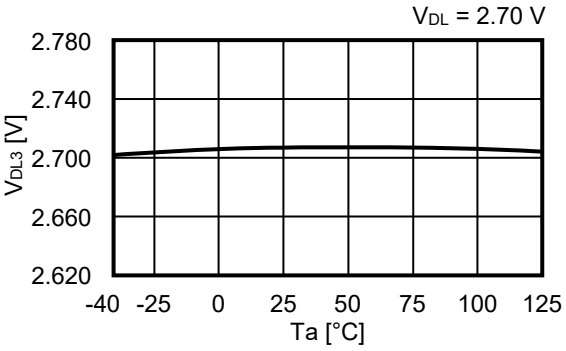
2. 13 V_{DL1} vs. Ta



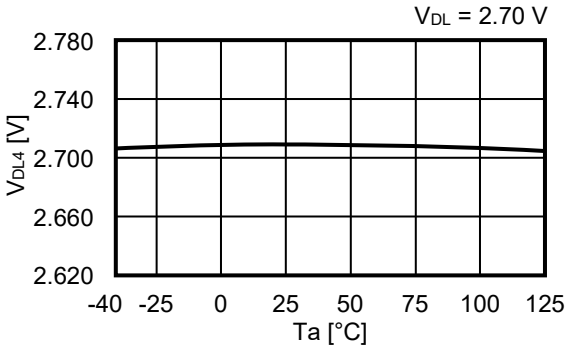
2. 14 V_{DL2} vs. Ta



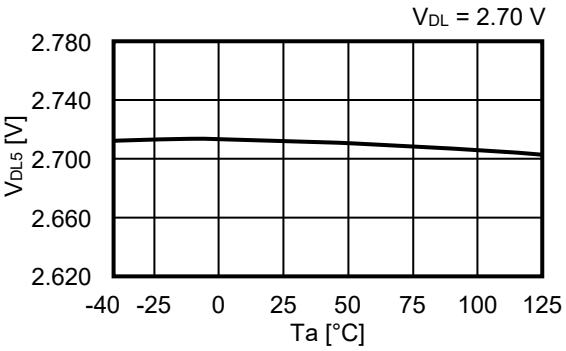
2. 15 V_{DL3} vs. Ta



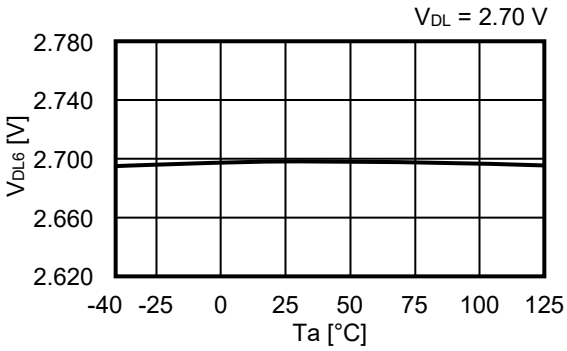
2. 16 V_{DL4} vs. Ta



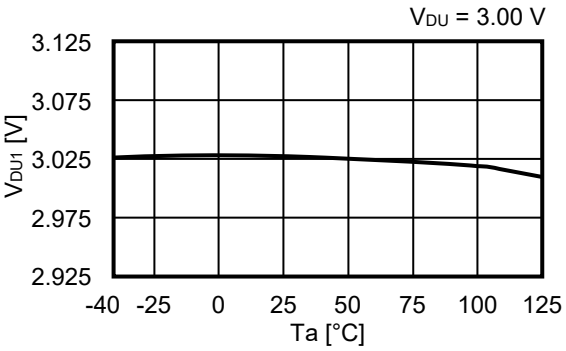
2. 17 V_{DL5} vs. Ta



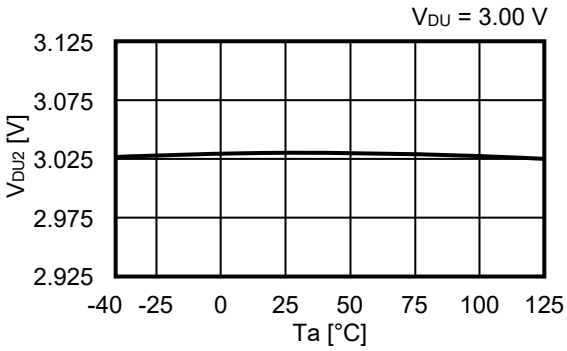
2. 18 V_{DL6} vs. Ta



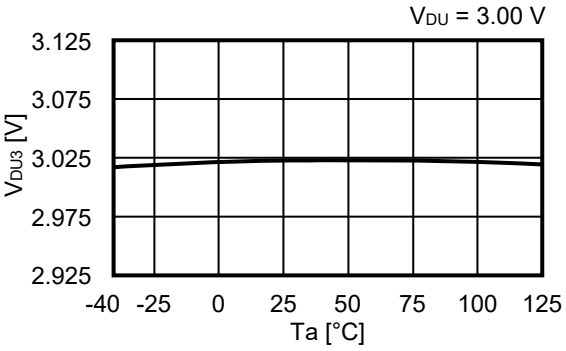
2. 19 V_{DU1} vs. Ta



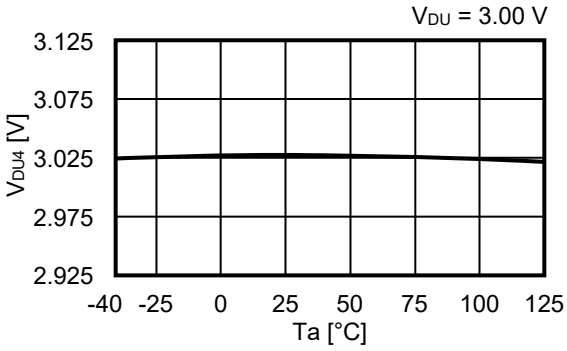
2. 20 V_{DU2} vs. Ta



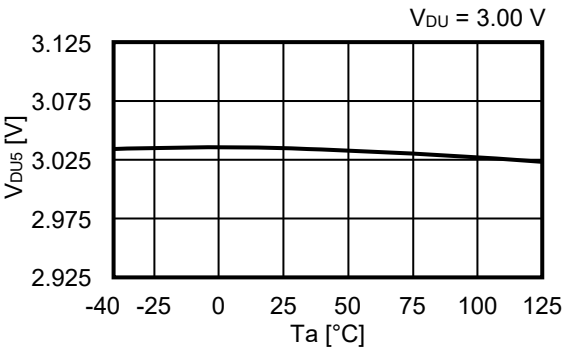
2. 21 V_{DU3} vs. Ta



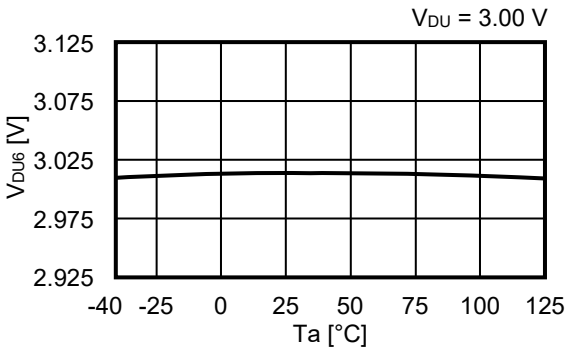
2. 22 V_{DU4} vs. Ta



2. 23 V_{DU5} vs. Ta

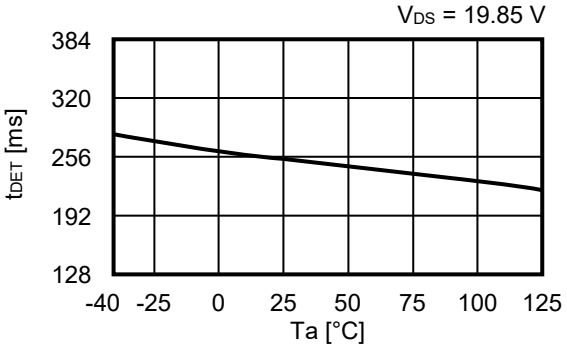


2. 24 V_{DU6} vs. Ta

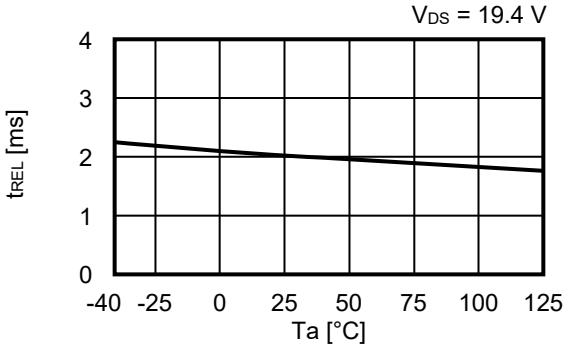


3. Delay time

3. 1 t_{DET} vs. Ta

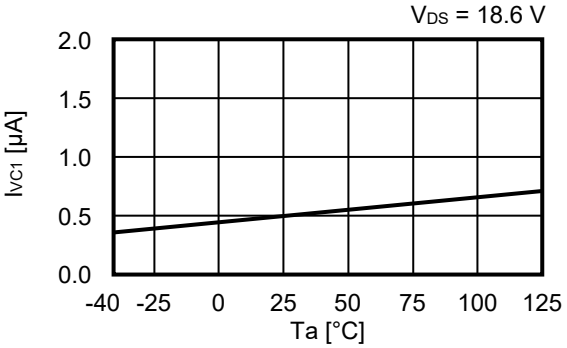


3. 2 t_{REL} vs. Ta

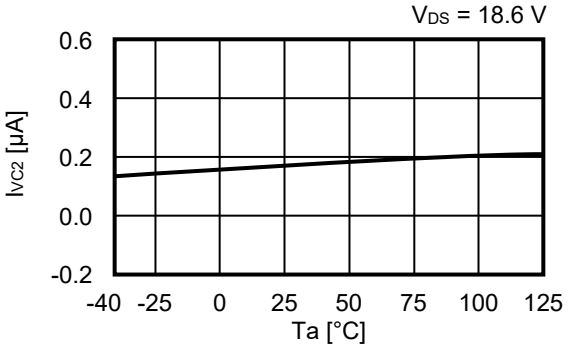


4. Input current

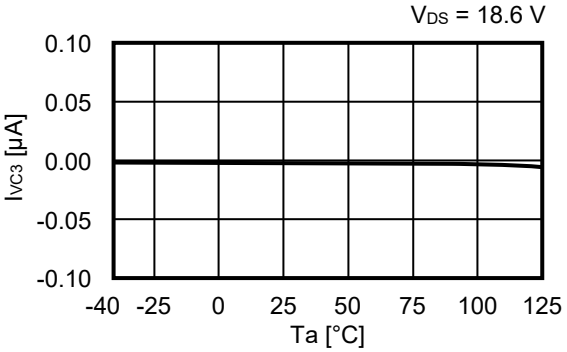
4. 1 I_{VC1} vs. Ta



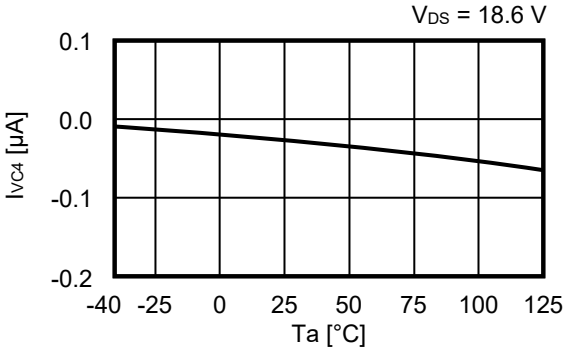
4. 2 I_{VC2} vs. Ta



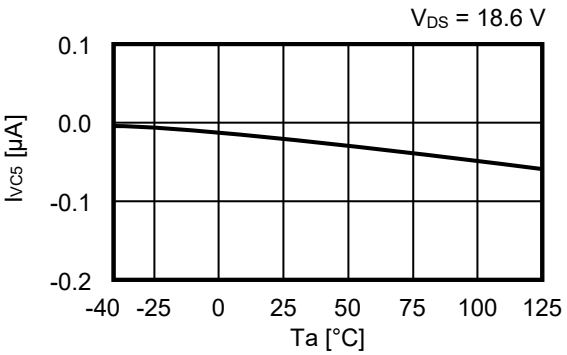
4. 3 I_{VC3} vs. Ta



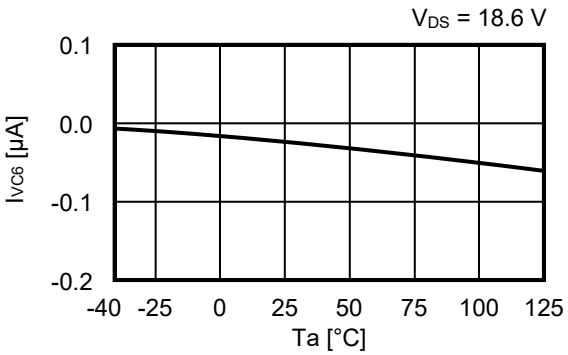
4. 4 I_{VC4} vs. Ta



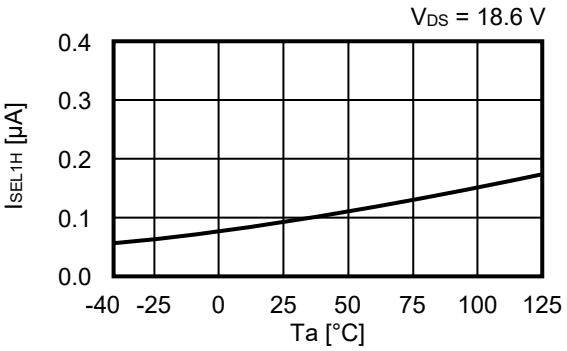
4. 5 I_{VC5} vs. Ta



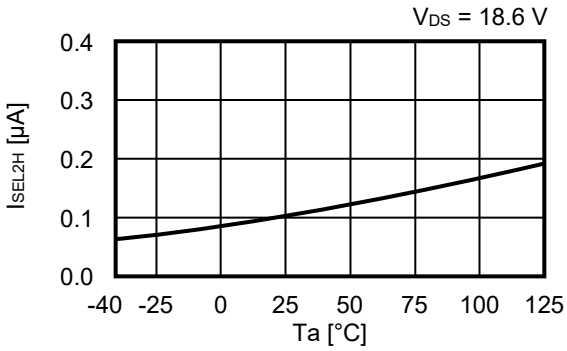
4. 6 I_{VC6} vs. Ta



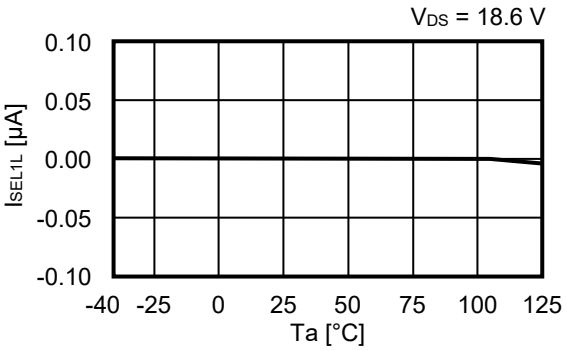
4. 7 I_{SEL1H} vs. Ta



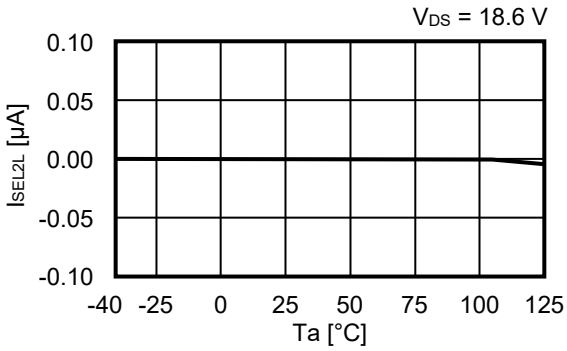
4. 8 I_{SEL2H} vs. Ta



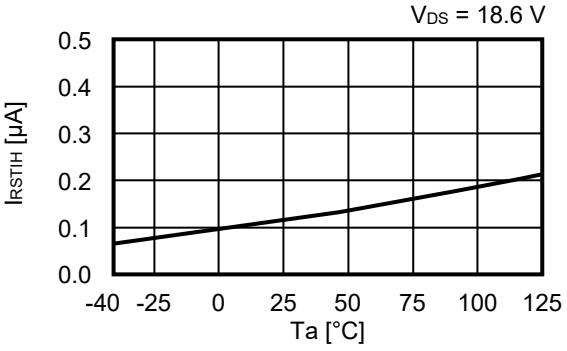
4. 9 I_{SEL1L} vs. Ta



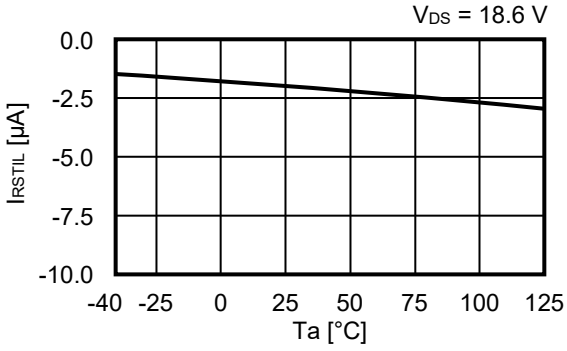
4. 10 I_{SEL2L} – vs. Ta



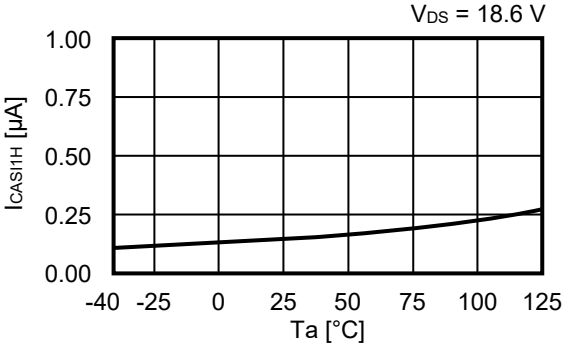
4. 11 I_{RSTIH} vs. Ta



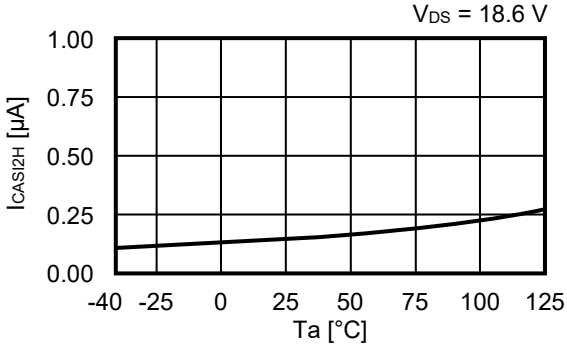
4. 12 I_{RSTIL} vs. Ta



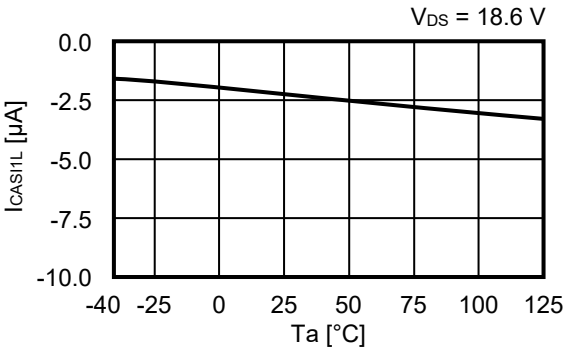
4. 13 I_{CASI1H} vs. Ta



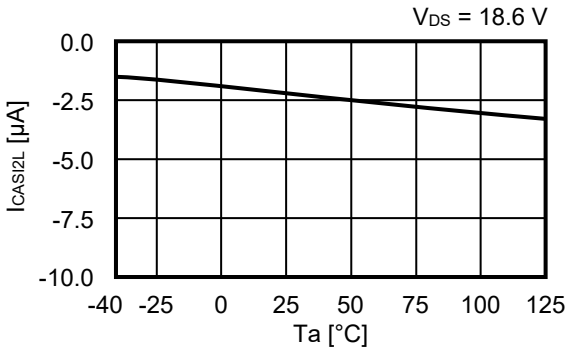
4. 14 I_{CASI2H} vs. Ta



4. 15 I_{CASI1L} vs. Ta

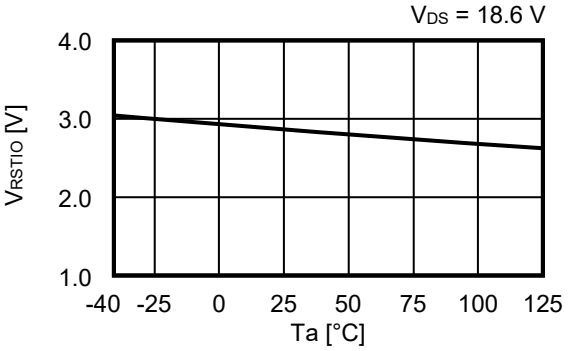


4. 16 I_{CASI2L} vs. Ta



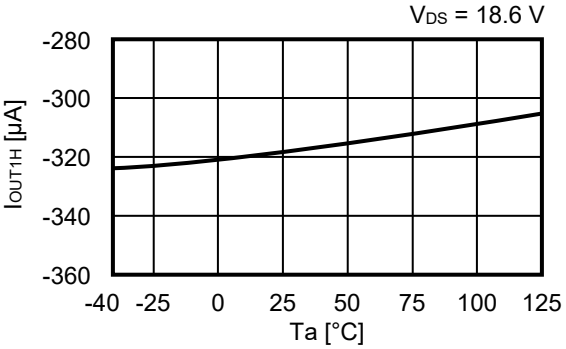
5. Output Voltage

5. 1 V_{RSTIO} vs. Ta

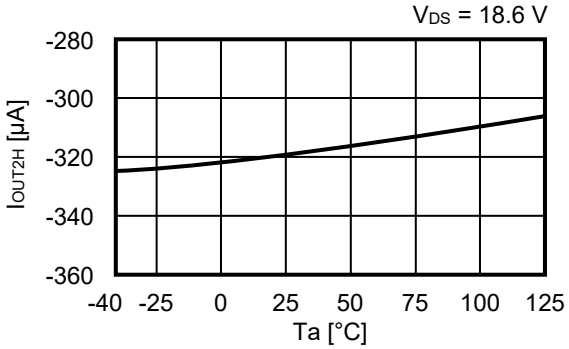


6. Output current

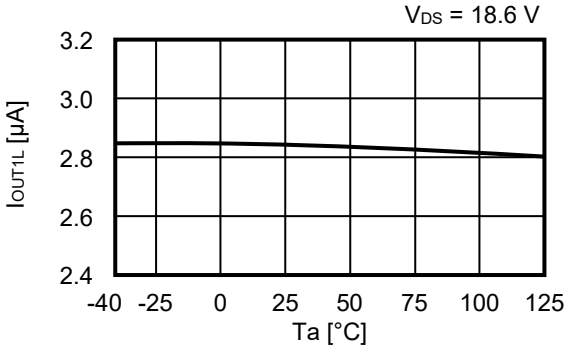
6. 1 I_{OUT1H} vs. Ta



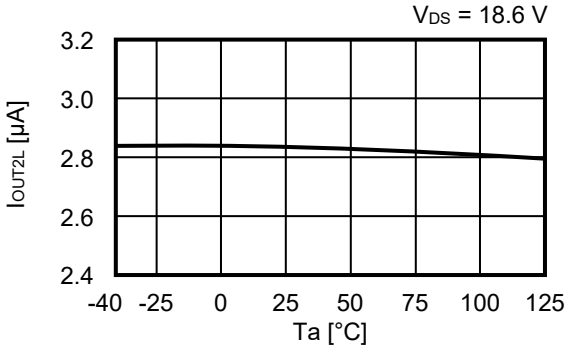
6. 2 I_{OUT2H} vs. Ta



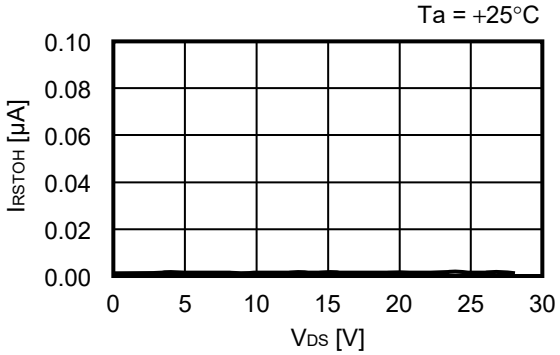
6. 3 I_{OUT1L} vs. Ta



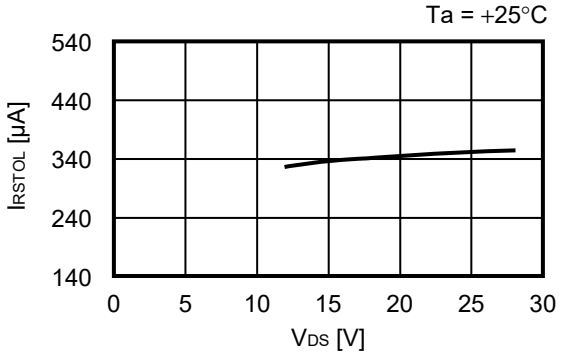
6. 4 I_{OUT2L} vs. Ta



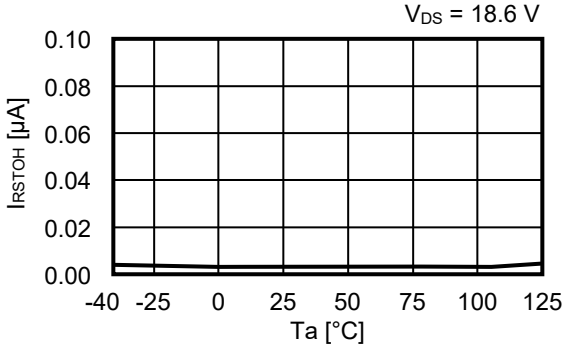
6. 5 I_{RSTOH} vs. V_{DS}



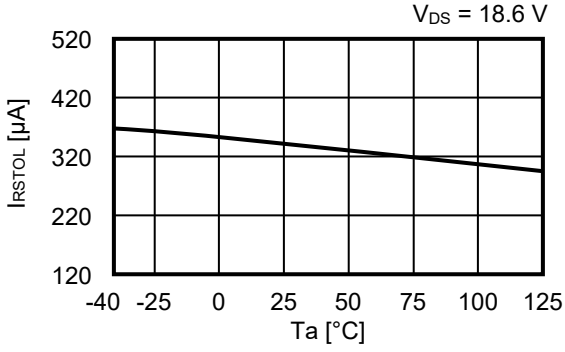
6. 6 I_{RSTOL} vs. V_{DS}



6. 7 I_{RSTOH} vs. Ta

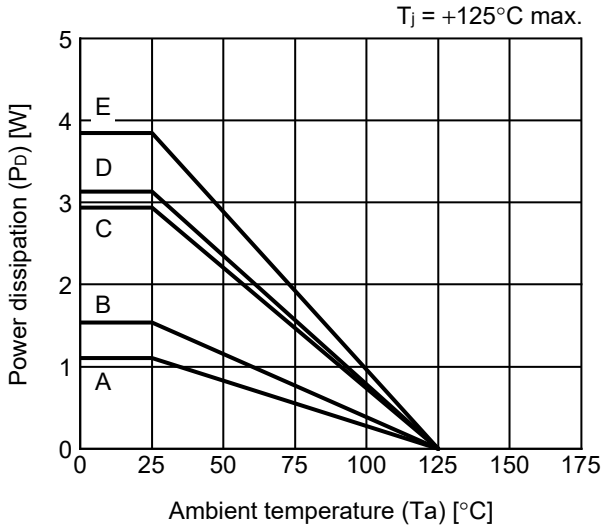


6. 8 I_{RSTOL} vs. Ta



■ Power Dissipation

HTSSOP-16

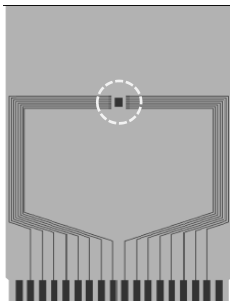


Board	Power Dissipation (P_D)
A	1.10 W
B	1.54 W
C	2.94 W
D	3.13 W
E	3.85 W

HTSSOP-16 Test Board

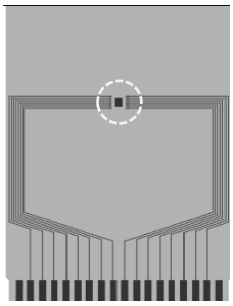
IC Mount Area

(1) Board A



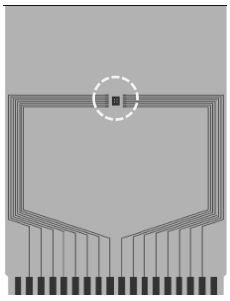
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

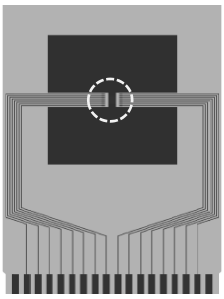
enlarged view

No. HTSSOP16-A-Board-SD-1.0

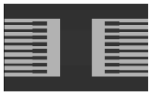
HTSSOP-16 Test Board

IC Mount Area

(4) Board D

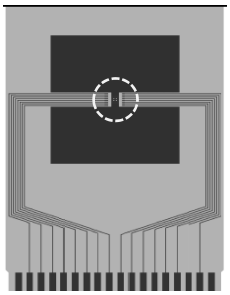


Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-



enlarged view

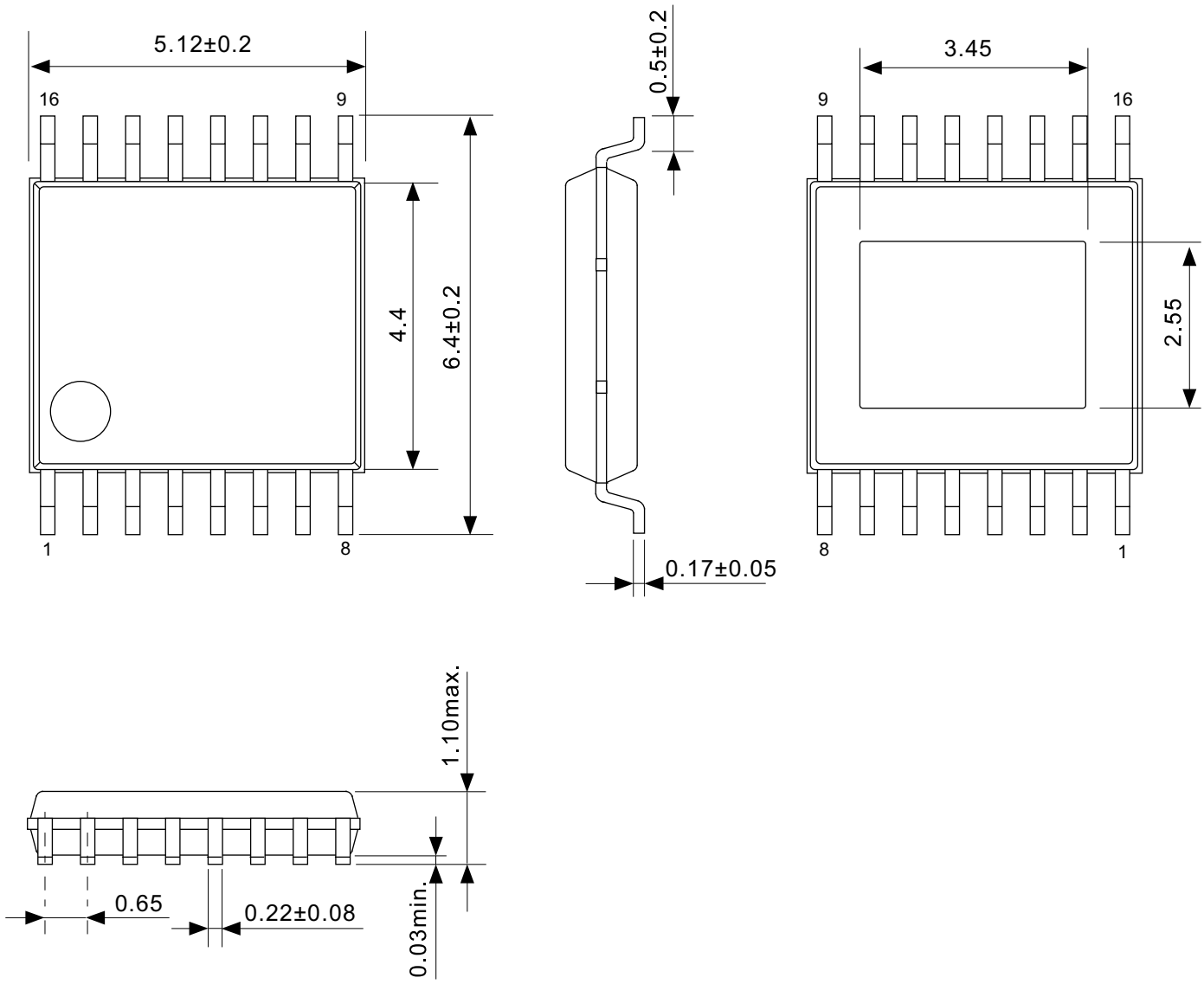
(5) Board E



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

enlarged view

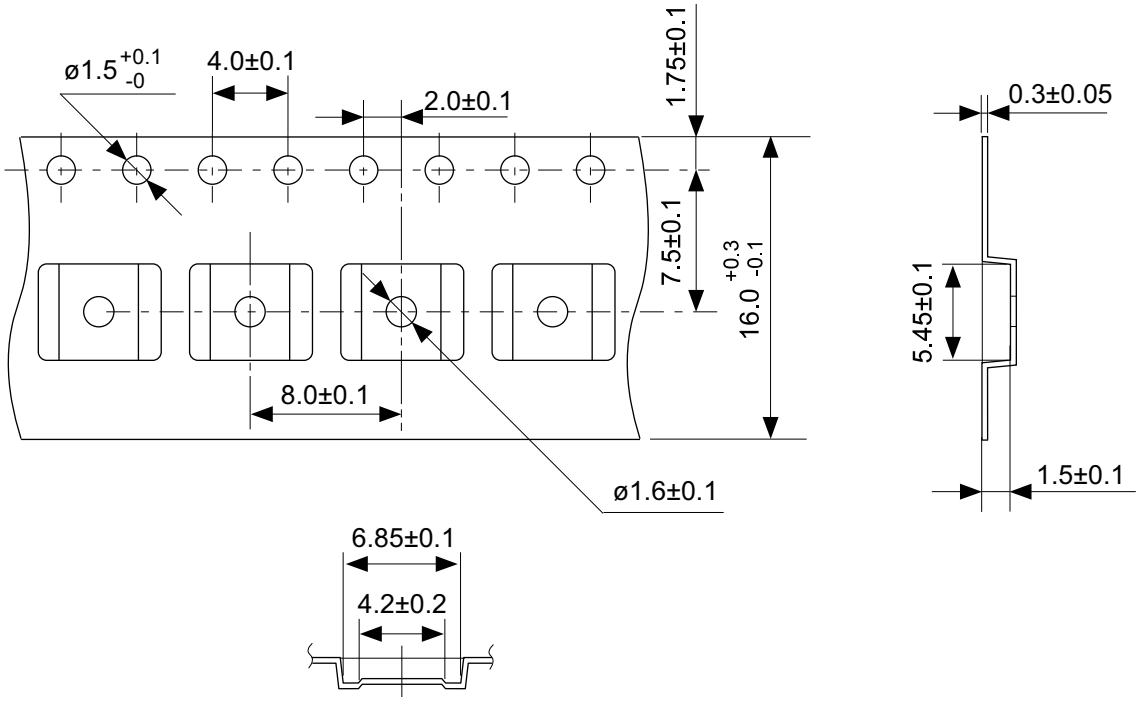
No. HTSSOP16-A-Board-SD-1.0

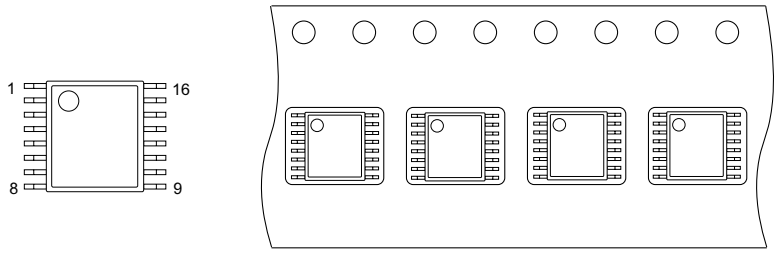


No. FR016-A-P-SD-1.0

TITLE	HTSSOP16-A-PKG Dimensions
No.	FR016-A-P-SD-1.0
ANGLE	
UNIT	mm

ABLIC Inc.



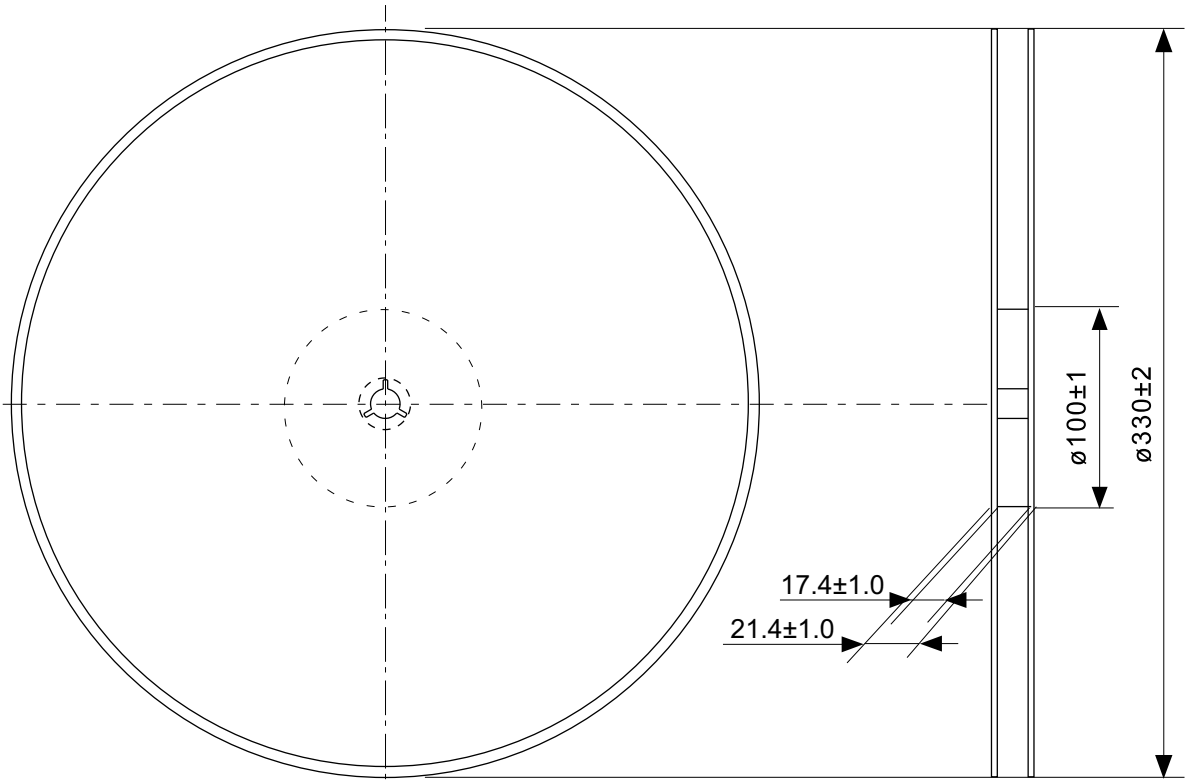


Feed direction

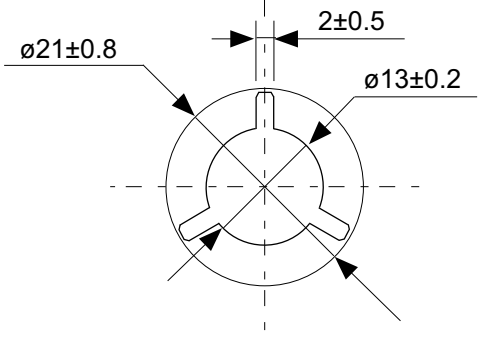
No. FR016-A-C-SD-1.0

TITLE	HTSSOP16-A-Carrier Tape
No.	FR016-A-C-SD-1.0
ANGLE	
UNIT	mm

ABLIC Inc.

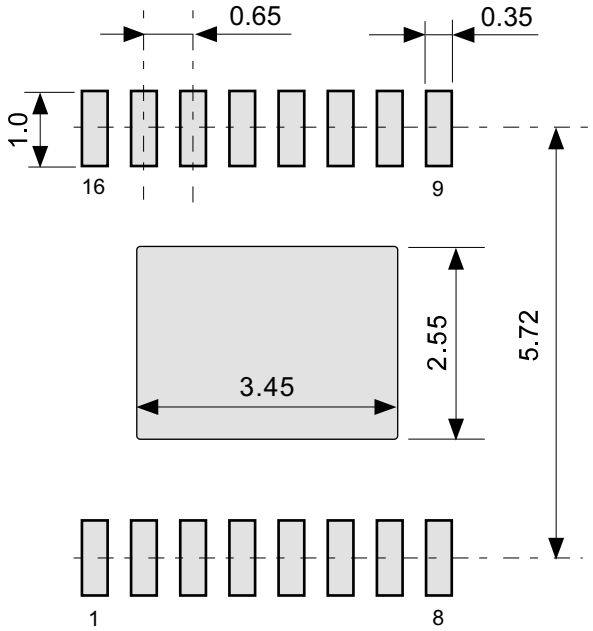


Enlarged drawing in the central part



No. FR016-A-R-SD-1.0

TITLE	HTSSOP16-A- Reel		
No.	FR016-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			



No. FR016-A-L-SD-1.0

TITLE	HTSSOP16-A -Land Recommendation
No.	FR016-A-L-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

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2.4-2019.07